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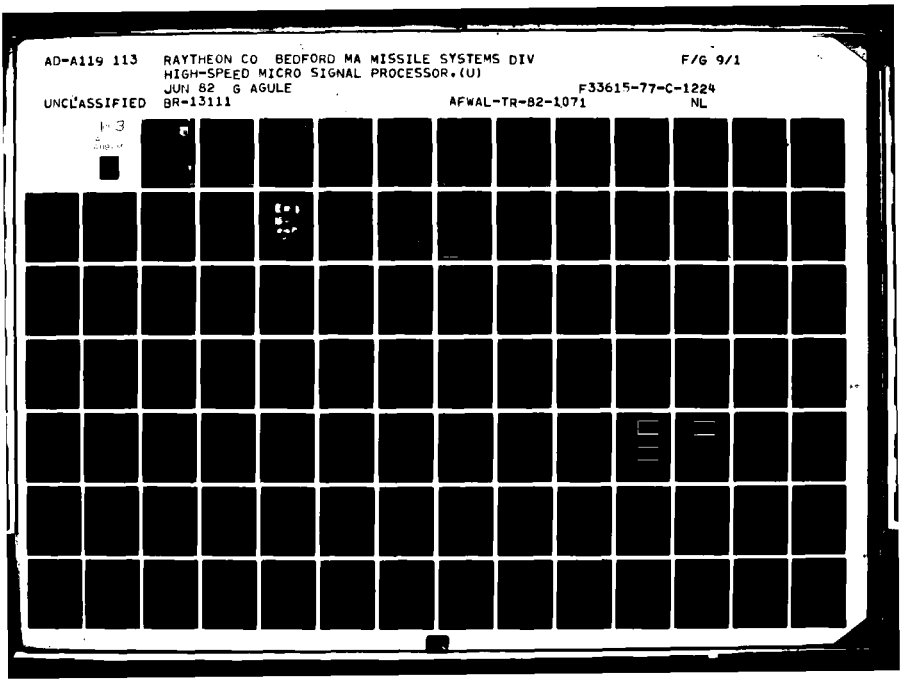

AD A119113

AFWAL-TR-82-1071

HIGH-SPEED MICRO SIGNAL PROCESSOR

George Agule

Raytheon Company
Missile Systems Division
Bedford Laboratories
Bedford, Massachusetts 01730

JUNE 1982

Final Report for Period 5 December 1977 - 30 December 1981

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THJS REPORT COVERS HARDWARE AND SOFTWARE TEST RESULTS OF CMOS/SOS LSI CHIPS AND A DEMONSTRATION UNIT PERFORMING A SELECTED SET OF SIGNAL PROCESSING ALGORITHMS. CHIP SPECIFICATIONS AND SYSTEM DESIGN DESCRIPTIONS ARE INCLUDED.

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1. PROGRAM OBJECTIVE

The objective of the High Speed Micro Signal Processor (HSMSP) program is to demonstrate the applications of programmable signal processor architecture and Complementary Metal Oxide Semiconductor/Silicon-On-Sapphire (CMOS/SOS) Large Scale Integration (LSI) technology to signal processing functions which previously have been implemented using a hard-wired approach. Examples of such functions include Fast Fourier Transforms (FFT), correlation, data sorting, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters, and Constant False Alarm Rate (CFAR) detection algorithms. The use of CMOS/SOS technology will allow these functions to be implemented using a single architecture whose throughput is comparable to that of the hard-wired approach, but whose power consumption and volume are only a fraction of that of the hard-wired unit.

2. PROGRAM SUMMARY

The HSMSP was divided into two phases; Phase I began in December of 1977 and ran until December of 1978, and Phase II ran from December of 1978 until completion.

The goals of Phase I were:

1) Design, fabricate, and test two Verification Processors, using T^2L technology
2) Generate a software package consisting of a Cross-Assembler and Monitor/Debug programs for the Verification Processors
3) Generate specifications for the CMOS/SOS LSI arrays to be used in the Demonstration Processor to be developed in Phase II

All of these goals were accomplished during the Phase I period with no significant problems. In addition, five more Verification Processors were built and delivered, and an improved Cross-Assembler-Simulator system was written and delivered along with a signal processor programming manual designed to cover both Verification and Demonstration Processors.

Phase II of the contract dealt with the detailed design, fabrication, and testing of the CMOS/SOS arrays to be used in the Demonstration Processor as well as the architectural definition, fabrication, and testing of the Demonstration Processor itself. The design goals of Phase II were to fabricate a single board processor with a micro-cycle clock rate of 6.6 megahertz (MHz). Also, firmware routines to demonstrate the functionality of the Demonstration Processor were coded and tested and modifications to the Monitor/Debug and Cross-Assembler system were made to accommodate the Demonstration Processor.

The two-phase program has been the basis of a major evolution in signal processing hardware as indicated in Figure 1. Developments at Raytheon have augmented the program to support specific applications in sonar, focal plane array lineaging, air to air missile seeker and LSI chip development. Common software (CLASP) has supported the program throughout.

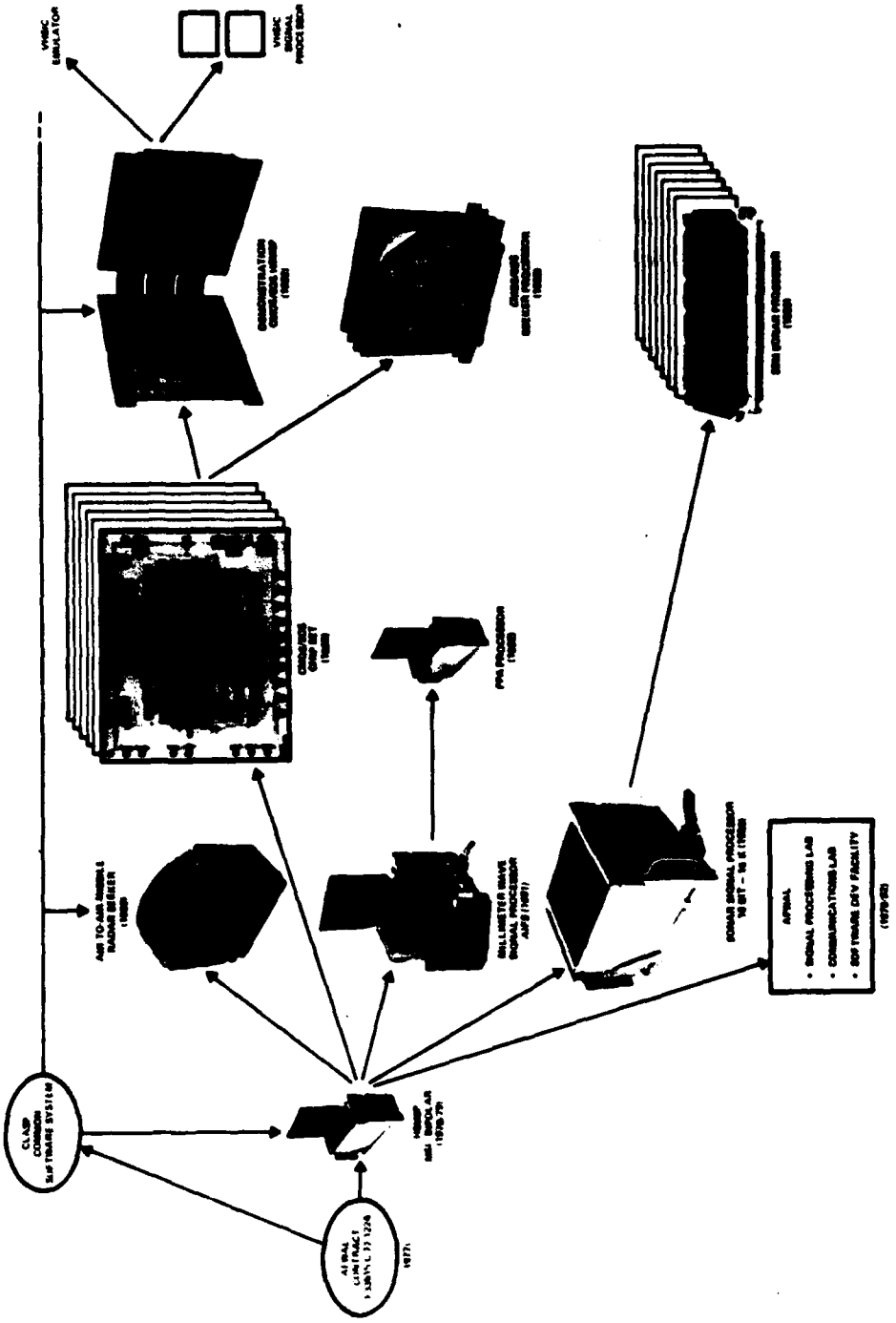


Figure 1 - High-Speed Micro Signal Processor (HSMSP) Evolving Signal Processing Technology

3. CMOS/SOS ARRAY DEVELOPMENT

Six CMOS/SOS LSI arrays were developed, fabricated, and tested for use in the Demonstration Processor. Three types were produced in conjunction with the Advanced Technology Laboratory of RCA Corp., and three were produced entirely by the Raytheon Microelectronics facility in Bedford. All six chips utilize five-micron technology and are designed to operate with a V_{DD} of 10 volts (V). The characteristics of the six arrays are summarized in Figure 2.

The three arrays developed by RCA employ custom logic cells and were interconnected manually to achieve a higher density of logic. The three Raytheon arrays use a set of standard logic cells and were interconnected automatically using the Multi-Port 2 Dimensional (MP2D) Router.

3.1 Array Descriptions

The following sections give a brief description of each array. More detailed information on each array is given in Appendixes A through F.

3.1.1 TCS140 Multiplier

The TCS140 is a two-clock delay, 12-bit by 12-bit binary multiplier that produces a 24 bit product in less than 150 nanoseconds (nsec). The multiplier design allows signed and unsigned arguments to be handled depending on control inputs in a basic 2's complement arithmetic number scheme for single and double precision operations.

The array consists of five separate logic groups, namely, two retiming registers, a decoding and partial adder, a final adder, and output tristate drivers.

The input arguments to the multiplier are the Multiplier, MULTB, and the multiplicand MULTA.

Two bits, SCA or SCB, control the signs of the two arguments. Other inputs are the system clock and a tristate enable for the product bits. The output consists of a 24 bit product with redundant sign bit.

DEVICE	DEVELOPED BY	GATES	CHIP SIZE	SPEED	CHARACTERISTICS
MULTIPLIER TCS140	RCA/ RAYTHEON	1300	233 x 190	< 150 ns	12 x 12 2's COMPLEMENT MULTIPLY
MULTIPORT/FIFO TCS142	RCA/ RAYTHEON	1000	230 x 173	< 90 ns ACCESS	16 WORD x 12 BIT 2 PORT ARRAY WITH FIFO LOGIC
SCALER TCS143	RCA/ RAYTHEON	1200	214 x 206	< 150 ns CYCLE	SCALING AND NORMALIZING OPERATION
REGISTER/ INTERFACE RB917	RAYTHEON	700	300 x 300	SUPPORT 150 ns CYCLE	TIMING/INTERFACE/GENERAL PURPOSE MULTIPLEXING
MSPALU RB918	RAYTHEON	1100	300 x 300	< 100 ns CYCLE	BIT SLICE RALU (8 BIT)
2909M (CMOS/SOS) RB919	RAYTHEON	600	220 x 180	< 90 ns CYCLE	BIT SLICE SEQUENCER (4 BIT) 16 WORD STACK

Figure 2 - μSP CMOS/SOS Logic Chips

A single multiplier is used in the arithmetic pipeline. Complex multiply is performed in four clock cycles.

A block diagram is shown in Figure 3.

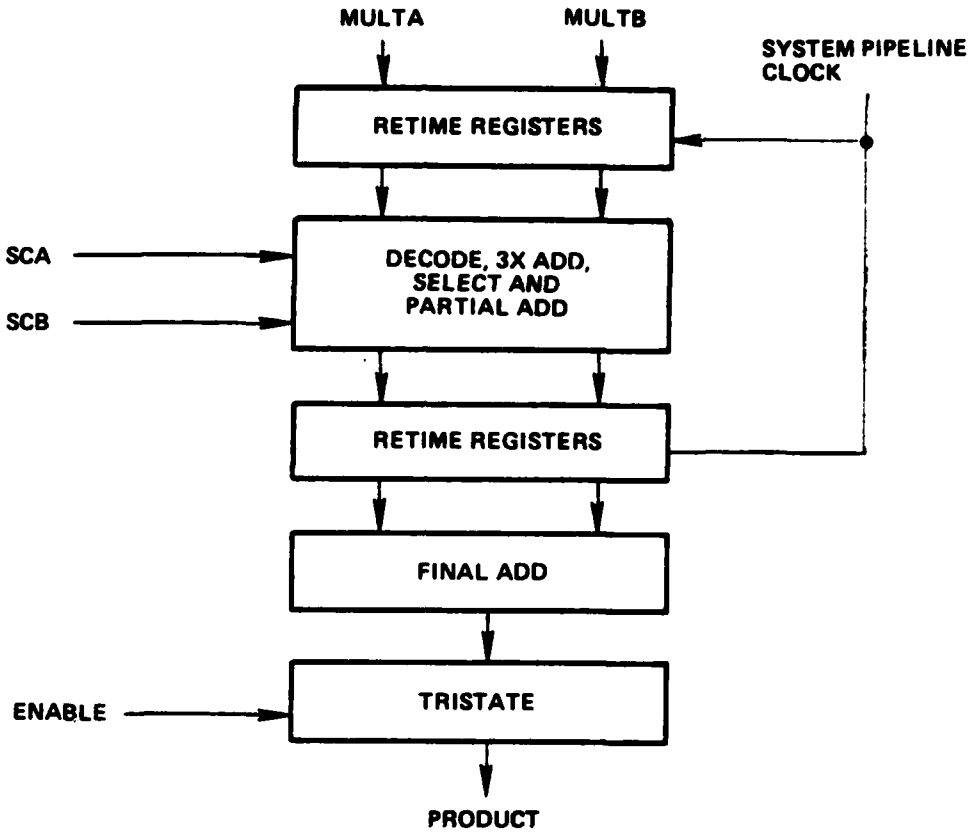


Figure 3 - TCS140 12 Bit x 12 Bit Multiplier Functional Block Diagram

3.1.2 TCS142 Multiport/FIFO

The TCS142 Multiport/FIFO array serves a dual role in the Micro Signal Processor. By external selection the array functions either as a multiport random access memory (RAM) or as a first-in-first out memory (FIFO).

A generalized block diagram of the TCS142, illustrated in Figure 4, shows how this selection is accomplished. When the FIFO select signal (FSL) is ONE, the FIFO mode of operation is selected and the A address and write address are generated by the

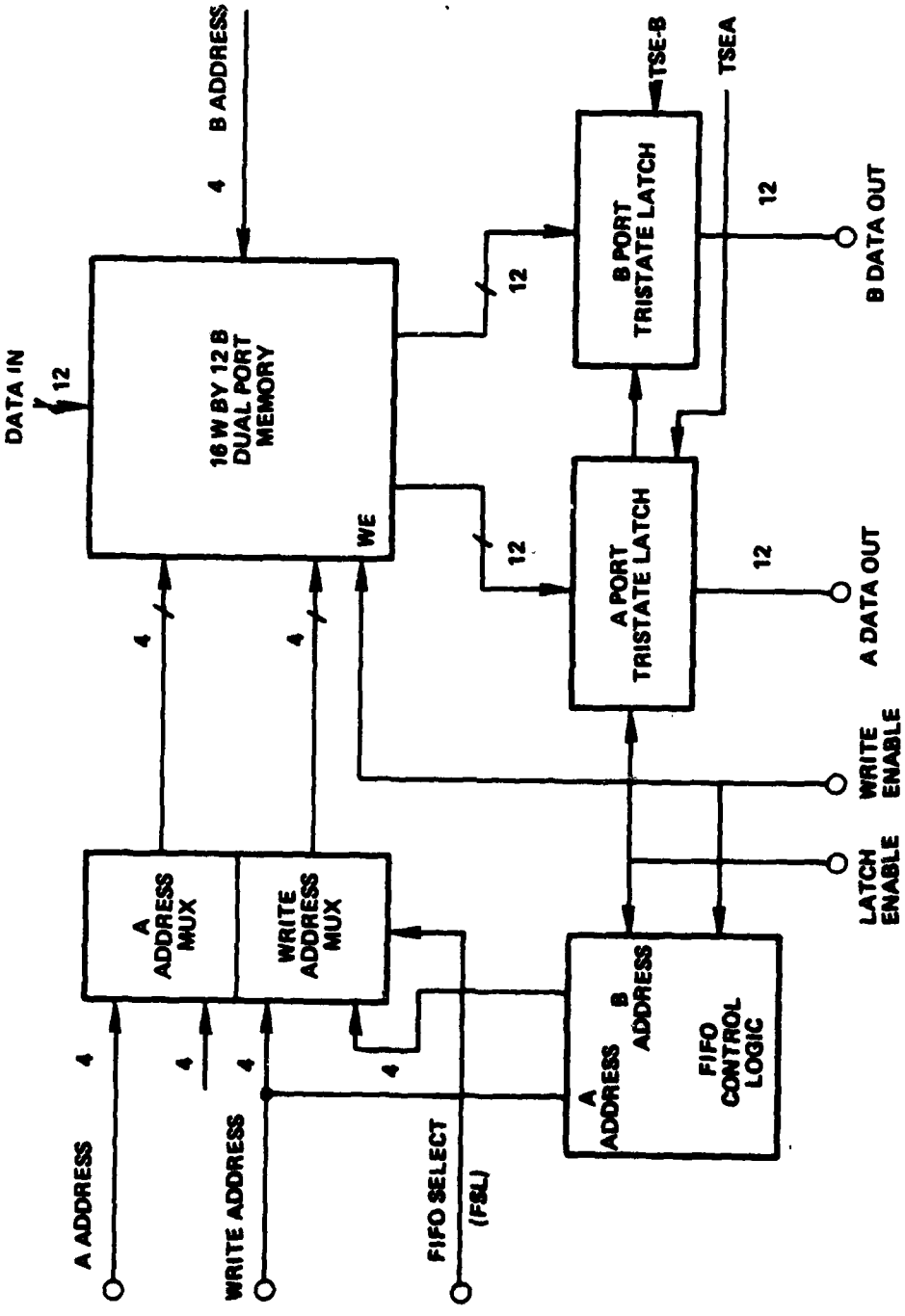


Figure 4 - TCS142 Multiport FIFO Block Diagram

FIFO control logic. When FSL = 0, the Multiport mode of operation is selected, and the A address and write address are generated external to the array.

The array itself is 12 bits wide by 16 words deep. The output of the array is latched to provide for same cycle reads and writes. The outputs of both ports are tri-stated to allow for expansion to deeper memories. In the FIFO mode, the TCS142 is parallel expandable to provide FIFOs that are multiples of 16 deep.

3.1.3 TCS143 Scaler/Shifter

The scaler/barrel shifter LSI array, also known as the TCS143, performs several scaling and data manipulations under microcode control. The array can shift (scale) 12 bits of input data based on either exponent (floating point), leading zero count (fixed), an external shift factor, or combinations of these factors.

The functions of the TCS143 can be subdivided into five logical blocks as follows:

1) Order memory to hold and reorder incoming data, while the appropriate shifts are being calculated.
2) Lead zero count logic to complete the number of leading zeros in the incoming data.
3) Scale register logic which operates on either the leading zero count or exponent, or both, to determine the largest number in a given set of numbers. Based on these operations, scale factors are generated to be used by the shift count generator.
4) Shift count generator which produces the shift count using the scale factors produced by the scale register logic and scale factors externally supplied.
5) The shift barrel which scales the data and/or strips the exponents from the magnitude.

A block diagram is shown in Figure 5.

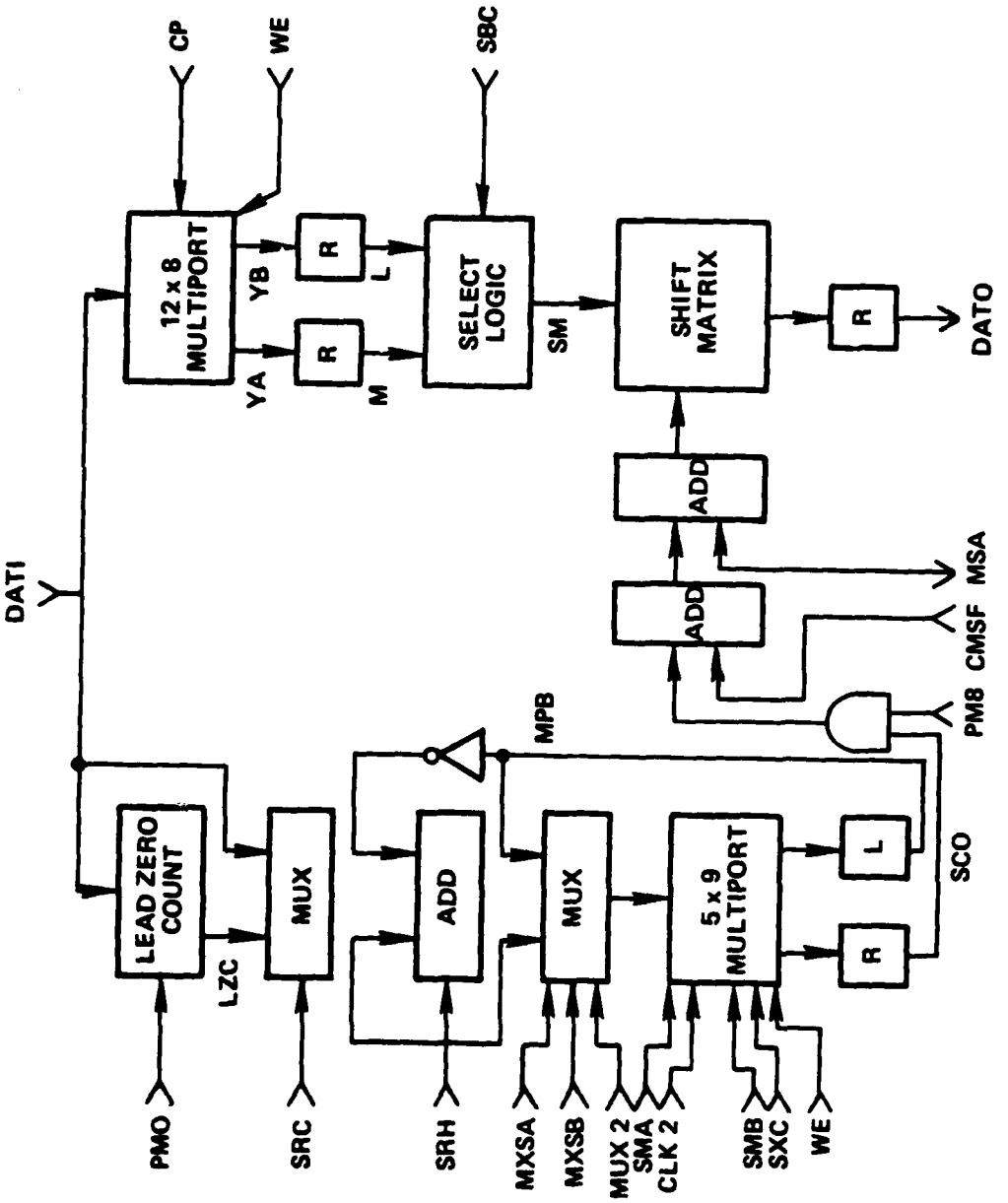


Figure 5 - TCS143 Pipeline Scale Chip Block Diagram

3.1.4 RB917 Register/Interface

The Register/Interface (R/I) array performs several functions on the Micro Signal Processor. The functions include the following:

1) Register Storage
2) Multiplexing
3) CMOS/SOS to T^2L Level Conversion
4) T^2L to CMOS/SOS Level Conversion
5) Data Memory Auto-Increment Counter
6) SSI Gates for Decoding, etc.
7) System Clock Generation

The requirement for level conversion occurs frequently in the Micro Signal Processor because of the use of T^2L memory. Today's technology requires the use of memories which are not 10 V SOS compatible.

Figure 6 shows the functional block diagram of the entire array. The tri-state enables determine which function a given chip performs. The Registers and Multiplexer have individual tristate and output voltage (power) pins. The first eight bit register serves as an eight bit general purpose counter, which will provide auto increment for data memory.

The SSI gates provide the logic required in various areas, such as pipeline microinstruction repeat/decode. These gates also provide a 'safety factor' to allow for potential minor design changes or flaws.

The timing logic provides most of the system clocks, as well as single step control.

3.1.5 RB918 MSPALU

The MSPALU is an eight-bit slice similar to a 2901, except that it performs several additional operations. The modifications are as follows:

- Separate write enable from latch enable.
- Provide output equal to the logical 'or' of data into the ALU right port.
- Allow direct input to S side of ALU.

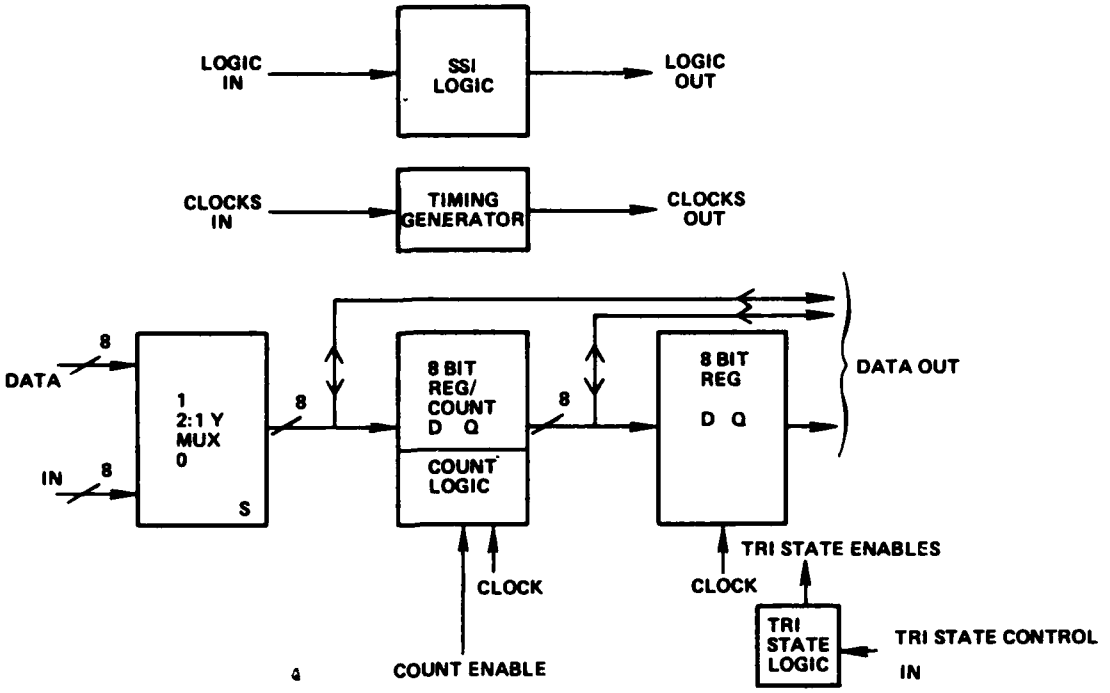


Figure 6 - RB917 Register/Interface Block Diagram

- Allow direct input to multiport.
- Provide separate write address, as well as two read addresses.
- Increased operating speed, especially multiport access.
- TTL compatibility (at 10 V operation) for certain input signals.
- Modified ALU operation as in Table 1.

TABLE 1

MODIFIED ALU OPERATIONS

Octal Code	Function	Symbol
0	R Plus S	R + S
1	S Minus R	S - R
2	R Minus S	R - S
3	R Or S	R $\vee$ S
4	R And S	R $\wedge$ S
5	R XOR X	R $\oplus$ S
6	R	R
7	S	S

A block diagram is shown in Figure 7.

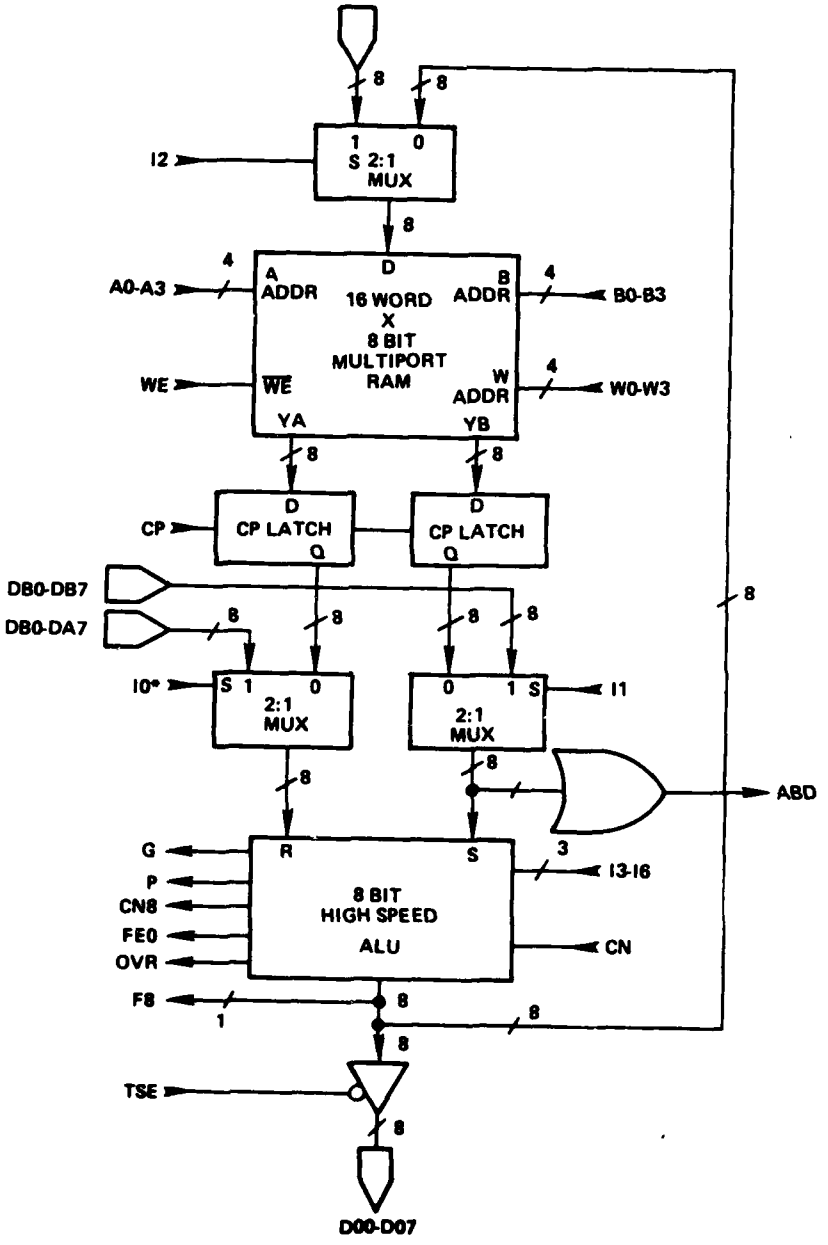


Figure 7 - RB918 MSPALU

3.1.6 RB919 2909M

The 2909M, shown in the block diagram in Figure 8, is functionally equivalent to the 2909 microprogram sequencer which is now commercially available in bi-polar technology. The difference is that the normal four word stack has been extended to 16 words in the 2909M, allowing for much more programming flexibility in the areas of interrupt handling and nested subroutines.

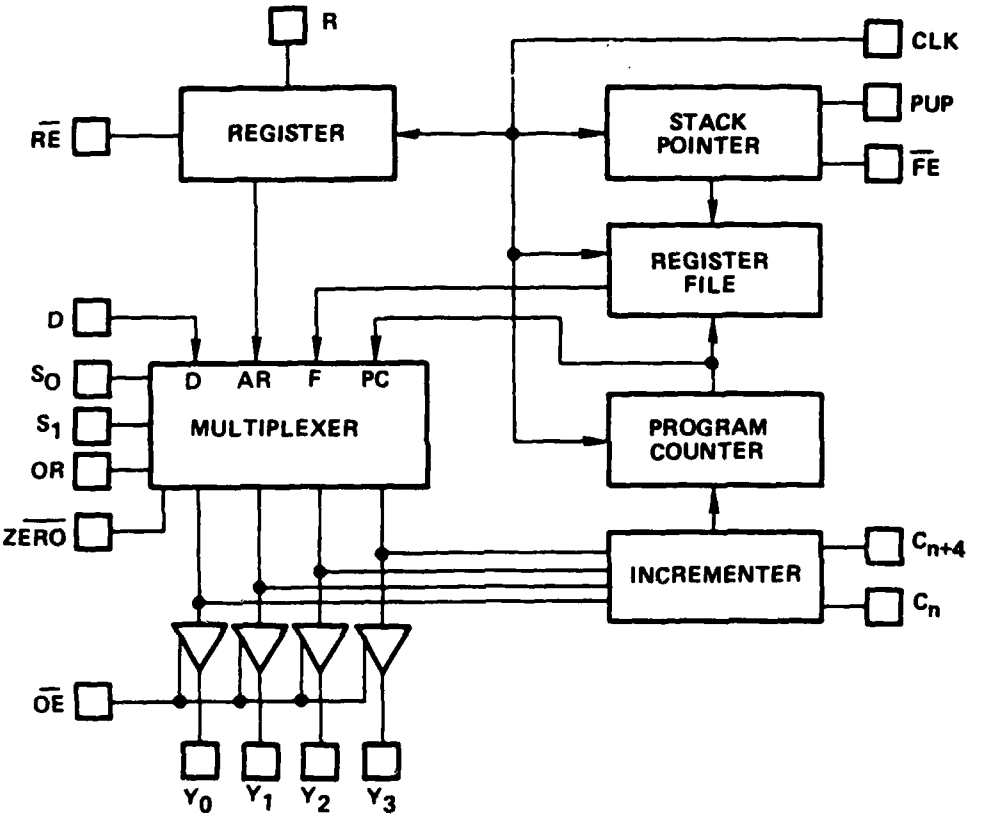


Figure 8 - RB919 (2909M) Block Diagram

The characteristics of the 2909M are:

- four-bit cascadable to any number of microwords
- Internal address register

- Branch input for N-way branches
- Cascadable four-bit microprogram counter
- 16 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock

3.1.7 Support Chips

In addition to the six LSI arrays, other functions were needed to complete the design of the Demonstration Processor, Specifically, these functions are:

1) High Density RAM
2) High Density Read Only Memory (ROM)
3) Level Shifting/Tristate Bus Interface
4) General SSI functions for Low-Speed I/O

The chip(s) used to fullfill these needs are described in the following sections.

3.1.7.1 2148H 1K x 4 Static RAM

The commercial Intel® 2148H 1K x 4 Static RAM was chosen to fill the requirement for high density RAM. The reasons for this choice are detailed in Section 4. The device itself is described in pages 1-41 to 1-44 of the 1981 Intel® "Component Data Catalog".

The devices are placed in 18 pin Leadless Chip Carriers (LCCs) by the Raytheon Hybrid Microelectronics facility for use on the Demonstration Processor. The LCC pinout is given in Figure 9.

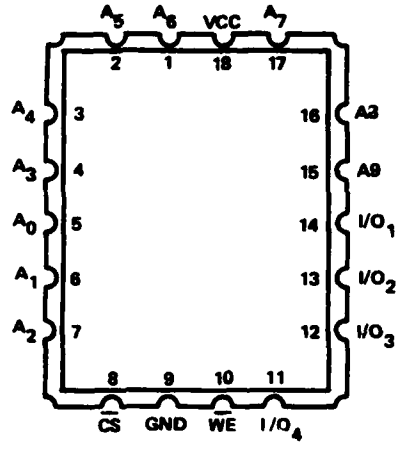


Figure 9 - 2148H LCC Pinout

3.1.7.2 RB930 16K Reconfigurable, Mask Programmable ROM

The Raytheon-developed 16K ROM with registered output was used to provide the pipeline micromemory and control decoding in the pipeline. This device has three configurations, selected by the state of certain I/O signals:

1) 512 W x 32 B
2) 1K W x 16 B
3) 2K W x 8 B

Eleven different personalizations were used in the Demonstration Processor. This device was packaged in a 64 pin LCC, and a pinout is shown in Figure 10.

3.1.7.3 RB916 8-Bit Bidirectional Level Shifter/Tristate Buffer

The RB916 is functionally equivalent to the bipolar 54/74LS245, described on pages 7-349 to 7-350 of the Texas Instruments "TTL Data Book for Design Engineers:.

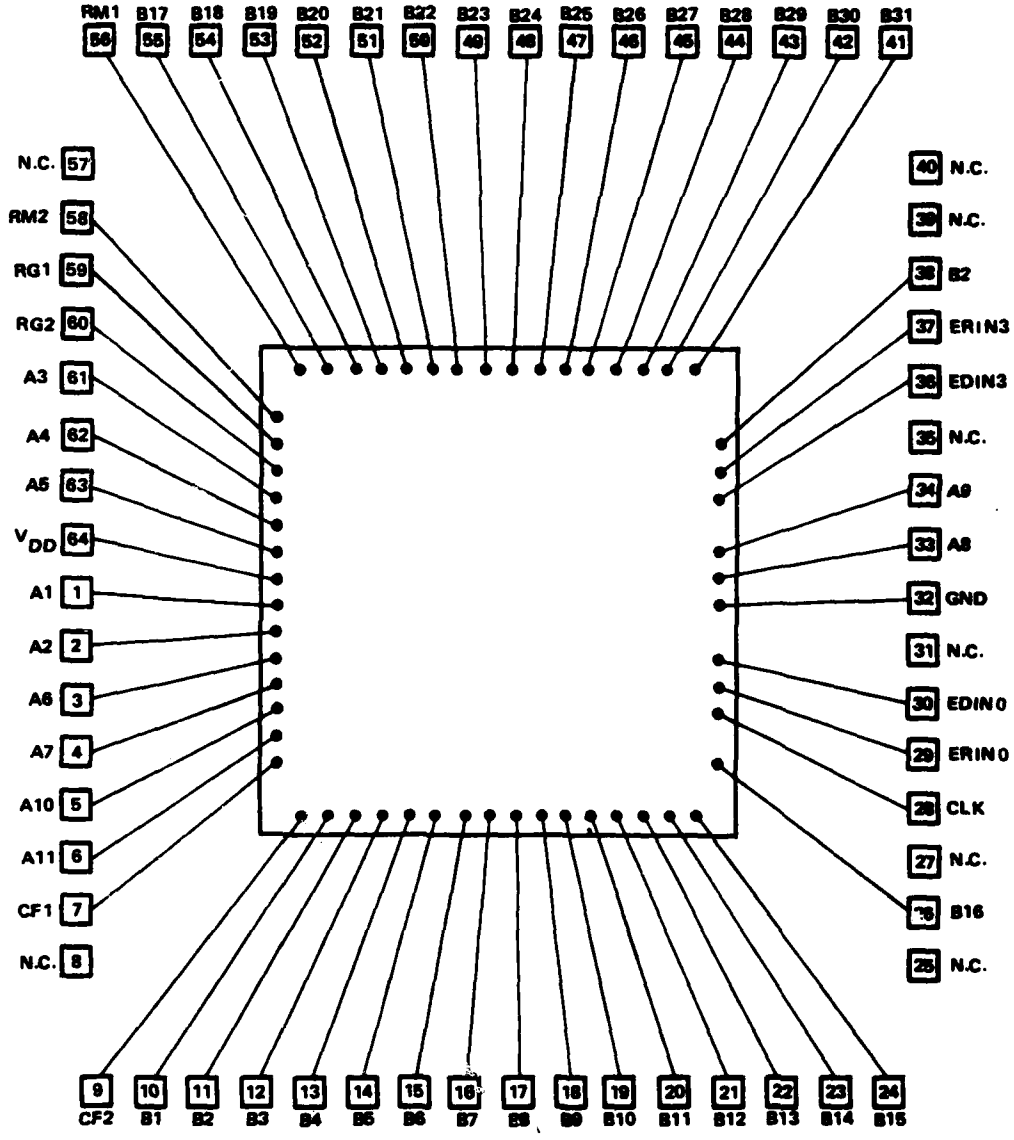


Figure 10 - RB930 (ROM) LLC Pinning

The RB916 is also capable of having the "A" and "B" inputs at different logic levels, under control of VA and VB inputs. This chip was used extensively to translate the 5 V outputs of the 2148H program memories to the 10 V levels of the rest of the system and also to provide diagnostic bus taps throughout the Demonstration Processor. The device was packaged in a 32 pin LCC, and a pin-out is given in Figure 11.

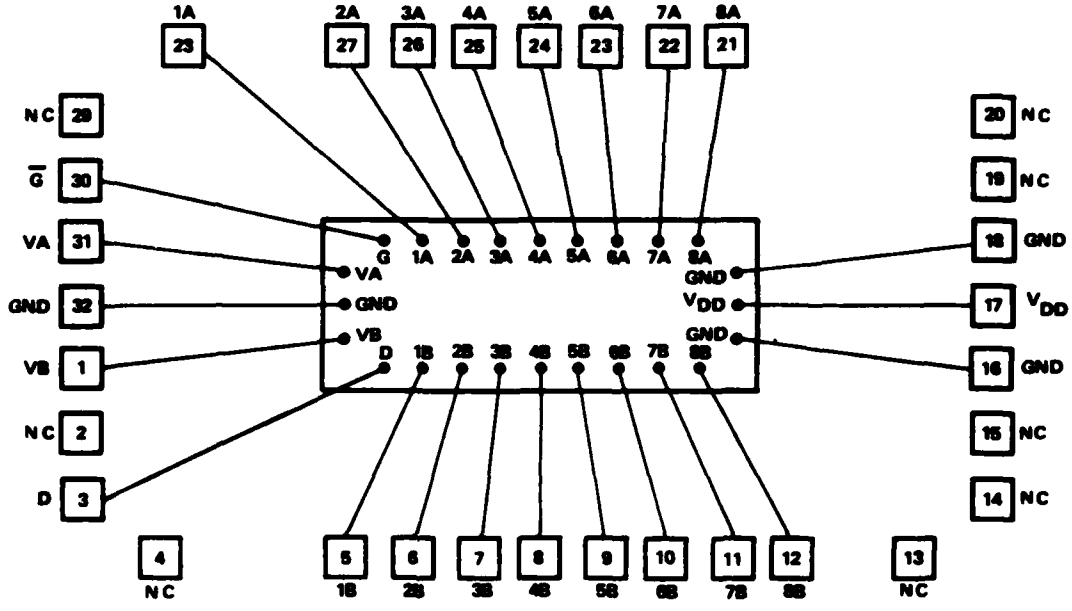


Figure 11 - RB916 LLC Pinning

3.1.7.4 General SSI Functions (Low Speed)

Six types of bulk CMOS, "4000" series integrated circuits were used in the design of the Demonstration Processor to implement the interface to the host PDP-11. The six types were:

1) CD4011B - Quad Dual-Input NAND Gate
2) CD4013B - Dual "D" FF with Set/Reset
3) CD4049UB - Hex Inverter
4) CD4073B - Triple 3 Input AND Gate
5) CD4081B - Quad 2 Input AND Gate
6) CD4515B - 4 to 16 Line Decoder

Data sheets on these devices can be found in the "RCA COS/MOS Integrated Circuits" data book. All but the CD4515B were packaged in 20 pin LCCs, with the CD4515B being packaged in a 24 pin LCC. Pinouts of these devices are given in Figures 12-17.

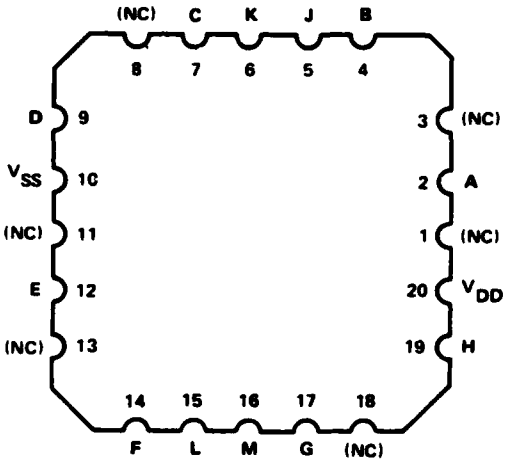


Figure 12 - CD4011B LCC Pinout

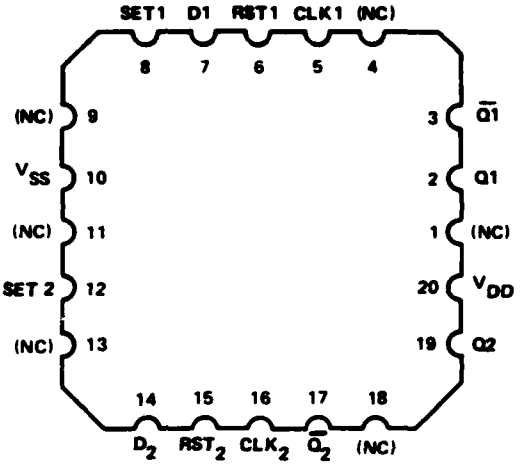


Figure 13 - CD4013B LCC Pinout

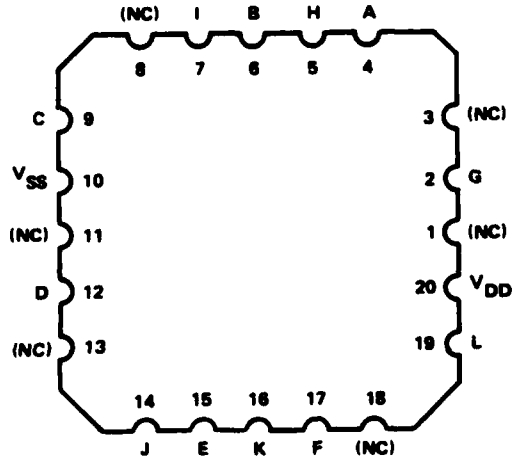


Figure 14 - CD4049UB LCC Pinout

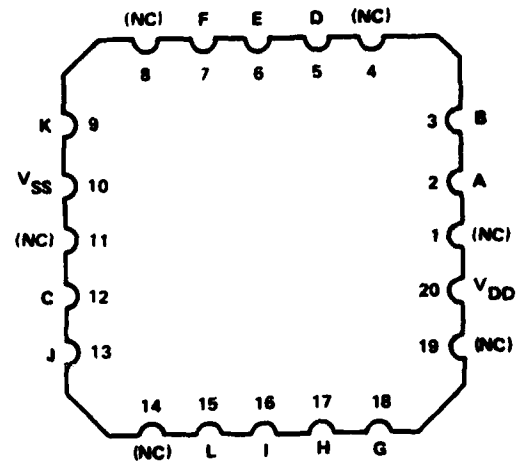


Figure 15 - CD4073B LCC Pinout

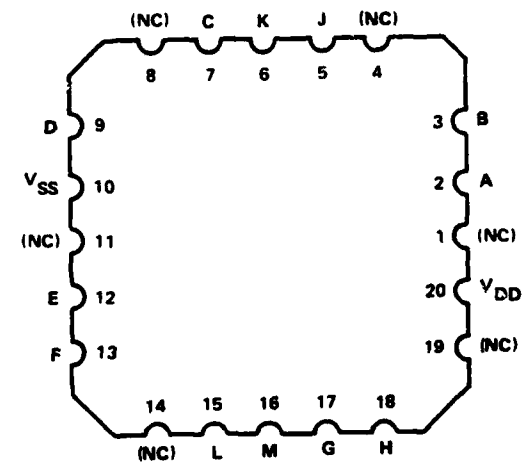


Figure 16 - CD4081B LCC Pinout

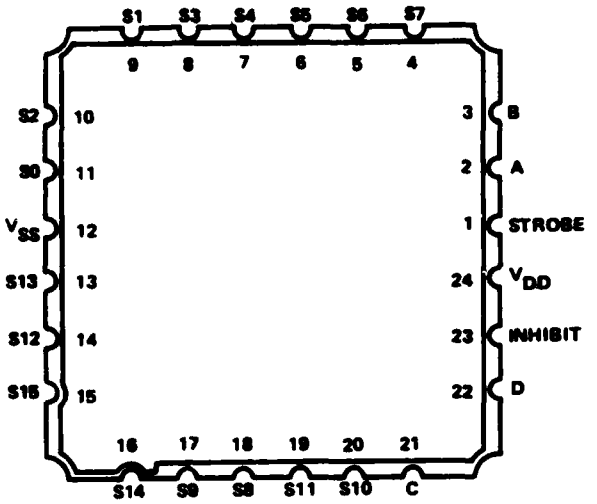
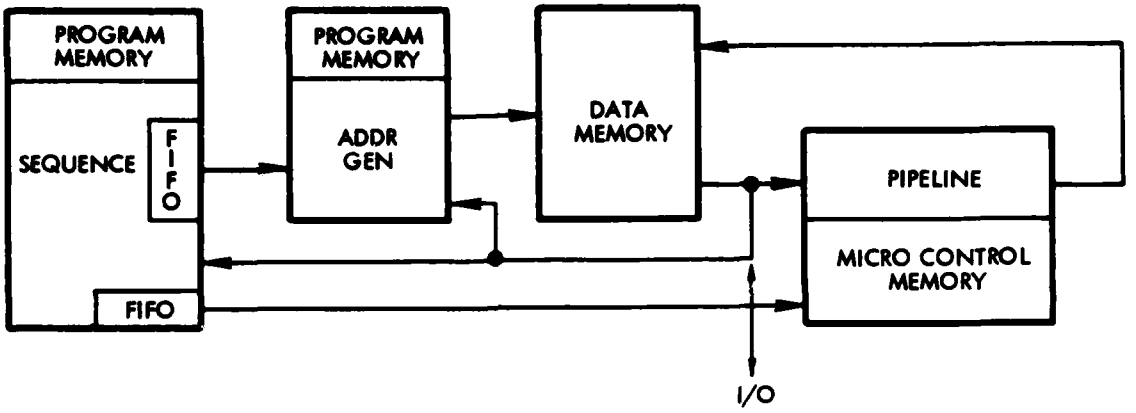


Figure 17 - CD4515B LCC Pinout

4. DEMONSTRATION PROCESSOR ARCHITECTURE

The Demonstration Micro Signal Processor utilizes the same basic four cycle architecture as the Verification Processors as shown in Figure 18. The functional areas of



- PROGRAMMABLE
- GENERAL PURPOSE
- HIGH THROUGHPUT
- FUNCTIONAL DEDICATION
- SEPARATE PROGRAM AND DATA MEMORIES

Figure 18 - Micro Signal Processor Architecture

Sequencer, Address Generator, Data Memory, and Pipeline have been maintained and their capabilities enhanced in the Demonstration Processor. A summary of the improvements is given in Table 2. These enhancements were gained at the expense of wider program memories in the Sequencer and ADGEN and a wider micromemory in the Pipeline. A comparison betwen the Verification and Demonstration Processor is shown in Table 3.

Functional descriptions of the Demonstration Processor Sequencer, ADGEN, and Pipeline are given in Volume I, Section 3, "Micro Signal Processor User's Guide", BR-12315-1. The only major difference between the Demonstration and Verification Sequencers is that the FIFO memory holding the ADGEN and Pipeline Macro calls has

TABLE 2

ARCHITECTURAL IMPROVEMENTS

Major Area	Demonstration	Verification
Pipeline:	1) 32 holding registers 2) 4 selectable flags 3) L↦R, R↦L ALU data transfer 4) Direct coefficient address input	1) 4 holding registers 2) 1 flag 3) - 4) -
ADGEN:	1) All 8 ALU functions allowed 2) 32 holding registers common to all 4 micro-cycles 3) Can use any one of four addresses in any order for write addresses	1) Only 2 ALU functions 2) 2 separate banks of 16 holding registers, 1 for first 2 micro-cycles, 1 for second 2 3) Limited to first and third cycles for first write, second and fourth cycles for second write
Sequencer:	1) 16 deep subroutine stack 2) All 8 ALU functions allowed	1) 4 deep surbroutine Stack 2) Only 4 ALU functions

TABLE 3

MEMORY WIDTH (IN BITS)

	T^2L Verification	CMOS/SOS Demonstration
Sequencer	48	55
ADGEN	24	32
Pipeline	44	72

been reduced from 64 to 16 words. Bit field definitions for the Sequencer and ADGEN program memories are given in Figure 19 through 22. Bit definition for the Pipeline micromemory are given in Volume II, Subsection 3.2.4.2, "Micro Signal Processor Programming Manual, BR-12315-2.

It should be emphasized that even though the Demonstration and Verification Processors execute different "primitive" instructions, any code written with the CLASP Cross Assembler system to run on the Verification Processor can also be run on the Demonstration Processor. The converse is not necessarily true because of the architectural enhancements added to Demonstration Processor.

The Demonstration Processor interface to the host PDP-11 is identical to that of the Verification Processors in theory of operation. More port codes have been added to the Demonstration Processor to account for the wider Sequencer and ADGEN program memories; also considerable hardware savings were obtained by making the Sequencer and ADGEN memory ports eight bits wide rather than the normal 12. The port codes for the Demonstration Processor are given in Table 4.

The Demonstration Processor also contains input and output FIFOs for high-speed data loading and unloading, and these are controlled in an identical manner to those in the Verification Processor. Special pipeline macro calls are used to control data flow from the input FIFO, data loading into the output FIFO, clearing both input and output FIFOs, and also generating DMA requests and using ADGEN outputs as input to the pipeline. These control codes are given in Figure 23. The only difference between Demonstration and Verification Processors is that the FIFOs in the Demonstration Processor have been shortened from 64 to 16 words.

At the time the Demonstration Processor design was finalized, no random access memory (RAM) capable of meeting the 150 nsec microcycle time and operating from a 10 V supply, was available.

It was decided to use a 5 V, 1K x 4 2148H memory device and use external level shifting devices (RB916s) to interface these memories to the rest of the Demonstration Processor. These memories are used in the Sequencer and ADGEN program memories, Data Memory, Coefficient, and Scale Factory memories. Pipeline micromemory was placed in mask-programmable CMOS/SOS ROM using the RB930. These ROMs were also used to provide control decoding in the pipeline.

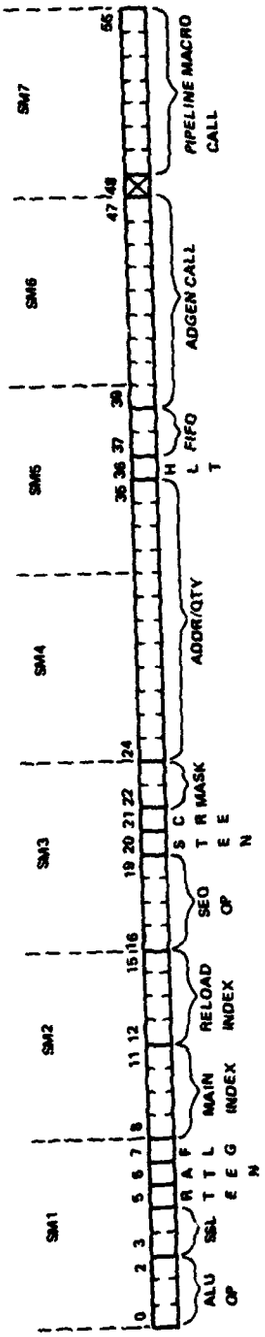


Figure 19 - CMOS/SOS SEQ Word Format

SEQ ALU OP A = RELOAD INDEX/NUMERIC 1
SEQ ALU OP B = SOURCE SELECTED BY SSL

SM0	01	02	-	MNEMONIC	FUNCTION	RESULT WRITTEN IN
0	0	0		ADD	A PLUS B	MAIN INDEX
0	0	1		BMA	B MINUS A	
0	1	0		AMB	A MINUS B	
0	1	1		AOB	A OR B	
1	0	0		AAB	A AND B	
1	0	1		XOR	A EX-OR B	
1	1	0		FEA	A	
1	1	1		FEB	B	

SSL - B SOURCE SELECT

SM03	04			
0	X	REG	SELECT MAIN INDEX AS B SOURCE	
1	1	QEN	SELECT QUANTITY FIELD AS B SOURCE	
1	0	XEN	SELECT EXTERNAL DATA AS B SOURCE	

RIE - RELOAD INDEX ENABLE
SELECT A SOURCE

SM05		
0	E	SELECT RELOAD INDEX AS A SOURCE
1	D	SELECT NUMBER 1 AS A SOURCE

ATTEN - ALU TEST ENABLE

SM06		
0	D	DISABLE
1	E	ENABLE TEST CONDITION ALU OVERRIDE

FLAG

SM07		
0	D	DISABLE
1	E	ENABLE FLAG

Figure 20 - CMOS/SOS SEQ Field Definitions (Sheet 1 of 4)

MAIN INDEX

SM08-SM11	MNEMONIC
0 0 0 0	C0
0 0 0 1	C1
0 0 1 0	C2
0 0 1 1	C3
0 1 0 0	C4
0 1 0 1	C5
0 1 1 0	C6
0 1 1 1	C7
1 0 0 0	C8
1 0 0 1	C9
1 0 1 0	C10
1 0 1 1	C11
1 1 0 0	C12
1 1 0 1	C13
1 1 1 0	C14
1 1 1 1	C15

RELOAD INDEX

SM12-SM15	MNEMONIC
0 0 0 0	C0
0 0 0 1	C1
0 0 1 0	C2
0 0 1 1	C3
0 1 0 0	C4
0 1 0 1	C5
0 1 1 0	C6
0 1 1 1	C7
1 0 0 0	C8
1 0 0 1	C9
1 0 1 0	C10
1 0 1 1	C11
1 1 0 0	C12
1 1 0 1	C13
1 1 1 0	C14
1 1 1 1	C15

Figure 20 - CMOS/SOS SEQ Field Definitions (Sheet 2 of 4)

SEQ OP-NEXT ADDRESS FUNCTION OP CODE

SM16	17	18	19		
0	0	0	0	POP	POP STACK & CONTINUE
0	0	0	1	PUSH	PUSH CURRENT ADDRESS ONTO STACK & CONTINUE
0	0	1	X	CONT	CONTINUE
0	1	0	0	POPAR	POP STACK AND JUMP TO ADDRESS IN AR
0	1	0	1	JSRAR	PUSH μPC, JUMP TO ADDR IN AR
0	1	1	X	JMPAR	JUMP TO ADDR IN AR
1	0	0	0	RTS	RETURN FROM SUBROUTINE, VIA TOP OF STACK
1	0	1	X	JMPSK	JUMP TO ADDR ON ON TOP OF STACK
1	1	0	0	POPQ	POP STACK, JUMP TO Q-FIELD ADDR
1	1	0	1	JSRQ	JUMP TO Q-FIELD ADDR, SAVE RETURN ADDR ON STACK
1	1	1	X	JMPQ	JUMP TO Q-FIELD ADDRESS

STEN - SEQ TEST ENABLE

SM20		
0	D	DISABLE
1	E	ENABLE TEST CONDITION SEQ OP OVERRIDE

CRE - ALU OP RESULT ENABLE

SM21		
0	E	ENABLE SEQ 2909 REG TO SAVE RESULT FROM ALU
1	D	HOLD PREVIOUS REGISTER CONTENTS

MASK - INTERRUPT MASK LEVEL

SM22	23		
0	0	L2	BOTH INTERRUPTS MASKED
0	1	L1B	INT2 (OUTPUT) UNMASKED
1	0	L1A	INT1 (INPUT) UNMASKED
1	1	L0	NEITHER INTERRUPT MASKED

Figure 20 - CMOS/SOS SEQ Field Definitions (Sheet 3 of 4)

SM24-35			ADDR/QUANTITY FIELD
			-2048 TO $+4095_{10}$, NOTE: POSITIVE VALUES 2047 MAP TO NEGATIVE VALUES
SM36			HALT
0	E		ENABLE HALT
1	D		DISABLE
SM37	**38**		FIFO
0	0	NV	NEVER LOAD FIFO
X	1	AL	ALWAYS LOAD FIFO
1	0	XT	LOAD FIFO CONDITIONALLY BASED ON TEST STATE
SM39-47			ADGEN CALL 0511_{10}
SM49-54			PIPELINE MACRO CALL $0-127_{10}$
SM48			SPARE

Figure 20 - CMOS/SOS SEQ Field Definitions (Sheet 4 of 4)

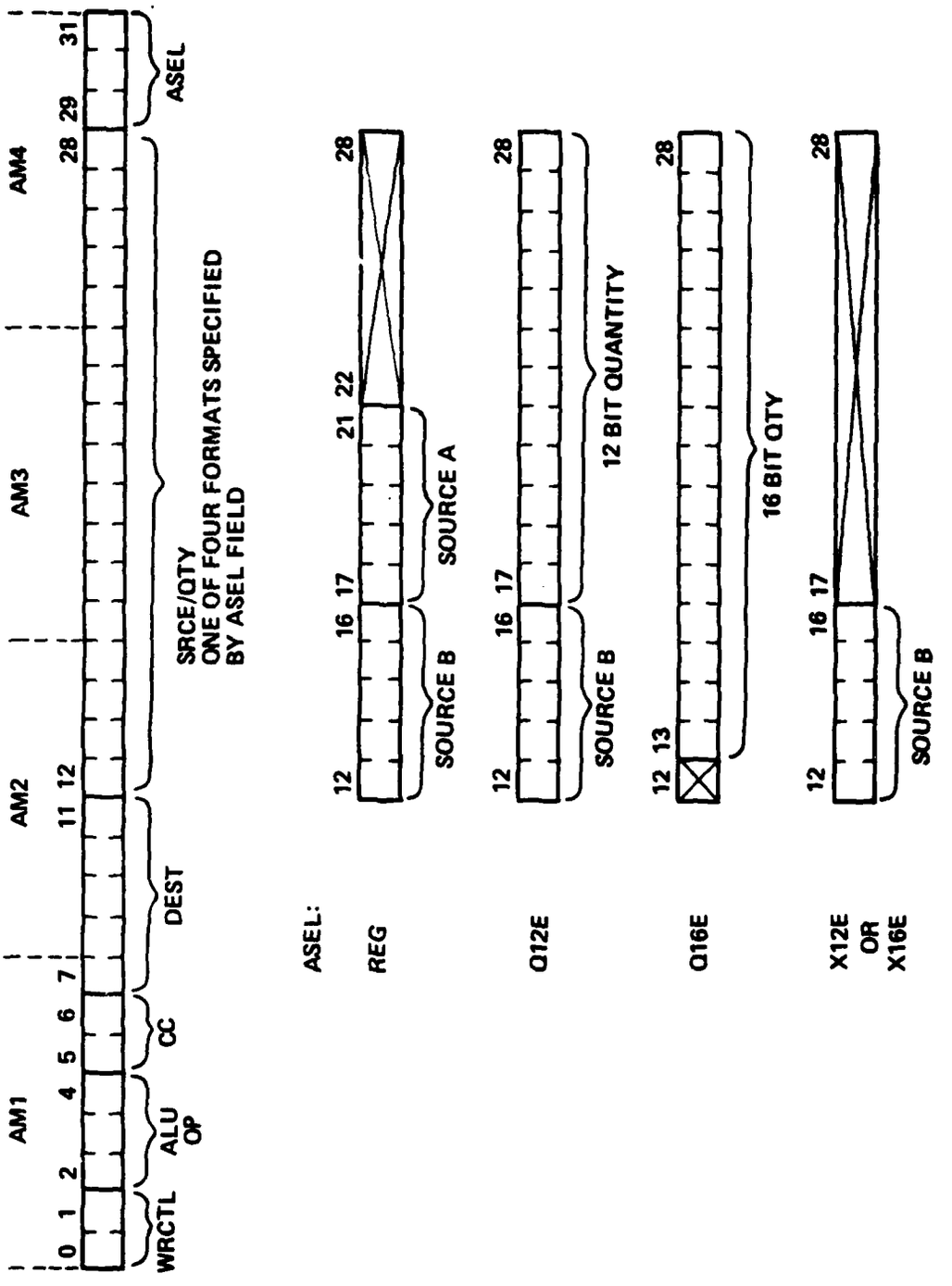


Figure 21 - CMOS/SOS ADGEN Word Format

WRCTL - Write Control

The WRCTL bits are multiplexed in time to control memory write options, and also a special coefficient option.

The field during cycle 0 is:

AM00	01	
0	0	C0 Write operand 1 data with cycle 0 address
0	1	C1 Write operand 1 data with cycle 1 address
1	0	C2 Write operand 1 data with cycle 2 address
1	1	C3 Write operand 1 data with cycle 3 address

The field during cycle 1 is:

AM00	01	
0	0	C0 Write operand 2 data with cycle 0 address
0	1	C1 Write operand 2 data with cycle 1 address
1	0	C2 Write operand 2 data with cycle 2 address
1	1	C3 Write operand 2 data with cycle 3 address

The field during cycle 2 is:

AM00	01	
1	X	WE1: E - Write operand 1 data with address specified in WR0P1
0	X	D - Do not write operand 1

Figure 22 - CMOS/SOS ADGEN Field Definitions (Sheet 1 of 5)

The field during cycle 3 is:

AM00	01			
E 1	0	D	WE2:	E - Write operand 2 data with address specified in WR0P2.
D 0	1	E		D - Do not write operand 2.
WE2	CFUNC		CFUNC:	E - Enable special coefficient function.
				D - Disable special coefficient function.

ALU OP B from reg file
A defined by ASEL

AM02	03	04	MNEMONIC	FUNCTION
0	0	0	ADD	A PLUS B
0	0	1	BMA	B MINUS A
0	1	0	AMB	A MINUS B
0	1	1	AOB	A OR B
1	0	0	AAB	A AND B
1	0	1	XOR	A EX-OR B
1	1	0	FEA	PASS A
1	1	1	FEB	PASS B

CARRY CONTROL

AM05		
0	D	Disable
1	E	Enable use of Carry-In F-F as Carry-In

AM06		
0	D	Hold old value
1	E	Allow new value into Carry-In FF

Figure 22 - CMOS/SOS ADGEN Field Definitions (Sheet 2 of 5)

AM07	08	09	10	11	DEST-
0	0	0	0	0	R0
0	0	0	0	1	R1
0	0	0	1	0	R2
0	0	0	1	1	R3
0	0	1	0	0	R4
0	0	1	0	1	R5
0	0	1	1	0	R6
0	0	1	1	1	R7
0	1	0	0	0	R8
0	1	0	0	1	R9
0	1	0	1	0	R10
0	1	0	1	1	R11
0	1	1	0	0	R12
0	1	1	0	1	R13
0	1	1	1	0	R14
0	1	1	1	1	R15
1	0	0	0	0	R16
1	0	0	0	1	R17
1	0	0	1	0	R18
1	0	0	1	1	R19
1	0	1	0	0	R20
1	0	1	0	1	R21
1	0	1	1	0	R22
1	0	1	1	1	R23
1	1	0	0	0	R24
1	1	0	0	1	R25
1	1	0	1	0	R26
1	1	0	1	1	R27
1	1	1	0	0	R28
1	1	1	0	1	R29
1	1	1	1	0	R30
1	1	1	1	1	R31

Figure 22 - CMOS/SOS ADGEN Field Definitions (Sheet 3 of 5)

AM12-28

SOURCE FIELD - A variable format field controlled by ASEL. This field supplies source code information for the ALU "A" and "B" operands.

If (ASEL = REG) then, two subfields.

SOURCE B - Address of register in the Register File to be used as the ALU "B" operand (see DEST field).

SOURCE A - Address of register in the Register File to be used as the ALU "A" operand (see DEST field).

Value - 0 to 31 numeric (for both).

If (ASEL = Q12E) then, two subfields.

SOURCE B - Address of register in Register File to be used as the ALU "B" operand (see DEST field).

Value - 0 to 31 numeric.

QUANT - 12 bit Quantity field to be used as the ALU "A" operand.

Value - $(-2048 \text{ to } +2047)_{10}$ numeric.

If (ASEL = Q16E) then, one subfield.

QUANT - 16 bit Quantity field to be used as the ALU "A" operand. No "B" operand is specified.

Value - $(-32768 \text{ to } +32767)_{10}$ numeric.

If (ASEL = X12E) or (ASEL = X16E) then, one subfield.

SOURCE B - Address of register in Register File to be used as the ALU "B" operand (see DEST field).

Figure 22 - CMOS/SOS ADGEN Field Definitions (Sheet 4 of 5)

Value - 0 to 31 numeric.

The "A" operand is External data, 12 or 16 bits depending on selection.

ASEL - A SOURCE SELECT

AM29	30	31		
0	0	X	REG	Enable reg file as "A" source
1	0	0	Q12E	Enable 12 bit quantity field as "A" source
1	0	1	Q16E	Enable 16 bit external data as "A" source
1	1	0	X12E	Enable 12 bit external data as "A" source
1	1	1	X16E	Enable 16 bit external data as "A" source

Figure 22 - CMOS/SOS ADGEN Field Definitions (Sheet 5 of 5)

TABLE 4

CMOS/SOS BUS ADDRESS ASSIGNMENTS

Bus In			Bus Out (Q = 0)			
			PORT = 0	OFI	Output FIFO	
Q = 1	SMR		1	SMR	Sequencer mar	
2	SM1		2	SM1	Sequencer mem	<0:7>
3	SM2		3	SM2	Sequencer mem	<8:15>
4	SM3		4	SM3	Sequencer mem	<16:23>
5	SM4		5	SM4	Sequencer mem	<24:31>
6	SM5		6	SM5	Sequencer mem	<32:39>
7	SM6		7	SM6	Sequencer mem	<40:47>
8	SM7		8	SM7	Sequencer mem	<48:54>
9	AMR		9	AMR	ADGEN mar	
10	AM1		10	AM1	ADGEN mem	<0;7>
11	AM2		11	AM2	ADGEN mem	<8:15>
12	AM3		12	AM3	ADGEN mem	<16:23>
13	AM4		13	AM4	ADGEN mem	<24:32>
14	DR1		14	DR1	Data mar	<0:3>
15	DR2		15	DR2	Data mar	<4:15>
16	DM1		16	DM1	Data mem (I)	<0:11>
17	DM2		17	DM2	Data mem (R)	<12:23>
18	CMR		18	CMR	Coefficient mar	
19	CFM		19	CFM	Coefficient mem	<0:11>
20	SCF		20	SCF	Scale Factor mem	<0:4>
21	CTL		21	VB1	Pipeline Input	<0:3>
22	INT		22	VB2	Pipeline Input	<4:15>
23	SP1		23	SCO	Shifter Output	
24	SP2		24	XXX	X-Multiplier Input	
25	SP3		25	YYY	Y-Multiplier Input	
26	SP4		26	BYP	Bypass Output	
27	SP5		27	ML1	Multiplier Output	<0:11>
28	SP6		28	ML2	Mulitplier Output	<12:23>
29	SP7		29	ALL	Left Pipeline ALU	
30	SP8		30	ALR	Right Pipeline ALU	
31	SP9		31	PLO	Pipeline Output	

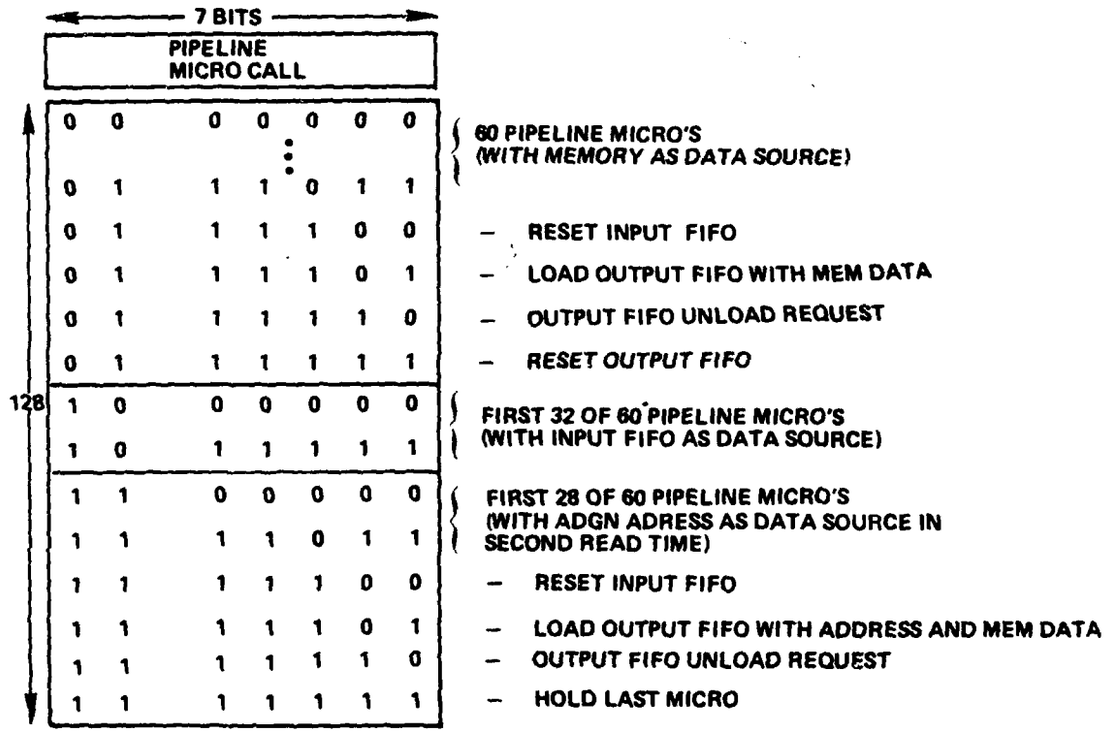


Figure 23 - Pipeline MACRO Control Codes

5. DEMONSTRATION PROCESSOR PACKAGING

The Demonstration Processor employs devices packaged in LCC mounted directly on a printed wiring board(s) (PWB). The PWBs were fabricated using a polyimide material, which closely matches the thermal coefficient of expansion of the ceramic used in the LCC and gives the advantage of higher packing density over dual-in-line packages (DIP), offering on the average a 4.65 to 1 improvement in area reduction. The savings in area are proportional to package size, and since the majority of Demonstration Processor devices has pin counts $\geq$ 32, the use of LCCs is particularly beneficial.

However, even with LCC packaging, the final device count of 248 ICs did not lend itself to the original concept of a single board Demonstration Processor. An alternate approach was taken, using two PWBs mounted back-to-back and connecting the two with flex cable to form a single assembly having one external I/O connector. The Demonstration Processor design was partitioned into two roughly equal (in terms of device area) parts: a Control board containing the system I/O, system timing, sequencer, and ADGEN and a Pipeline board containing the Pipeline, Data Memory, Coefficient memory, and scale factor memory. The physical dimensions of each board are 11 x 11 inches, and each board has a 14 layer construction. The Control Board contains 140 ICs, and the 140 pin system I/O connector and the Pipeline board contain the remaining 108 ICs. Three flex cables, with a total of 147 signals, interconnect the two boards.

6. TEST RESULTS

6.1 Array Testing

All six LSI arrays, as well as the RB916 and RB930 chips, were tested on either the Sentry VII or Sentry VIII test systems located in the Raytheon Microelectronics facility. The test programs for the three arrays developed by RCA were line-for-line translations of test programs used by RCA's in-house test system. The test programs developed for the Raytheon devices were generated as a by-product of the simulation program used in the computer aided design (CAD) progress. The 2909M (RB919) was also tested using a test program provided by Raytheon Semiconductor, Mountainview, CA., which manufactures the bipolar 2909. Two iterations were required on the Register/Interface (RB917) and the 2909M (RB919) before full functionality was achieved.

Speed and parametric data for the three RCA arrays are given in Appendixes D through F. Typical test data for RB916, RB917, RB918, RB919 and RB930 is given in Tables 5 through 9. The test data for the 2909M (RB919) also gives a comparison between the 2909M and its bipolar counterpart.

The test data indicates that internal gate delays for this family of five micron devices are on the order of three to five nsec, which compares favorably with those found in T^2L logic families. When going on and off chip, the high input and output impedance and low drive current of CMOS causes significant I/O delays on the order of 10-15 nsec. Thus, the minimum delay path through a CMOS/SOS chip has a set lower limit of 15-20 nsec. The comparison of the 2909M (RB919) and its T^2L (Table 9) counterpart bears out the conclusion that CMOS/SOS performs significantly better on the long internal paths of the circuit, but is less satisfactory where the gating level is less.

The most significant problem to surface during device testing was the logic thresholds on T^2L compatible inputs. The RB916 was the first chip to be produced employing these inputs and consequently had the worst problem. The logic zero threshold was found to be around 800 millivolt (mV) and the logic one threshold to be around 1200 mV at room temperature. The logic zero threshold was seen to drop as low as 200 mV at low temperatures. Design improvements were incorporated into the RB917 and RB918, and the

TABLE 5

RB916 BUS/INTERFACE PARAMETRIC CHARACTERIZATION

I_{DD}(mA) @V_{DD}=10 V	I_{DN}(mA) @V_O=0.5 V		I_{DP}(mA)	SOS		TTL	
				IIH(μA) @V_{IN}=10 V	IIL(μA) V_{IN}=0 V	IIH(μA) V_{IN}=5 V	IIL(μA) V_{IN}=0 V
9.0	10 V	5.4	-1.9				
	5 V	5.5	-1.7	-22	-16^5	-40	-16^5

Prop Delay (nsec)

A → B	20
B → A	20

TABLE 6

R/I (RB917) PARAMETER CHARACTERIZATION

Register Interface No. 917 High Speed Micro Signal Processor (CMOS/SOS) Program R.T. Parametric Characterization (Typical) Sample Size = 15 Devices						
			SOS		TTL	
IDD(mA) @ VDD=10 V	IDN(mA) @ V0=0.5 V	IDP(mA) @ V0=9.5 V	IIH(NA) @ V1N=10 V	IIL(NA) V1N=0 V	IIH(NA) V1n=5 V	IIL(μA) V1n=0 V
5 mA	3.2	-2.0	10	10	10	115

R.T. Dynamic Characterization (Critical Paths)

Signal Path Where [ ] = Signal Pin Numbers	Propagation Delay (nsec) typ @ CL 35 pF
[58] → [10] MUX (MA0) → Output (My0) Gating Levels = 10	$T_{P_{LH}}$ 32-40 $T_{P_{HL}}$ 37-47
[46] → [10] MUX (MXS, MX52) → Output My0) Gating Levels = 12	$T_{P_{LH}}$ 41-50 $T_{P_{HL}}$ 40-50
[60] → [12] (G1A,G1B) → G1Y Gating Level = 8 [62] → [14] (G2A,G2B) → G2Y Gating Level = 6 [1] → [16] (G3A,G3B) → G3Y Gating Level = 8 [5] → [20] (G4A,G4B) → G4Y Gating Level = 7	$T_{P_{HL}}$ 26-33 $T_{P_{LH}}$ 28-36 $T_{P_{LH}}$ 31-40 $T_{P_{HL}}$ 24-30
Register a Clock Output [19] → [15] CK2 → RA0 Gating Levels = 11	TA1 45-57

TABLE 7

RB918 MSPALU PARAMETRIC CHARACTERIZATION (TYPICAL)

IDD (MA) @ VDD = 10V	IDN (MA) @ VO = 0.5V	IDP (MA) @ VO = 9.5V	SOS		TTL	
			IIH (NA)	IIL (NA)	IIL (UA)	IIL (UA)
15.4	2.75	-4.13	2.8	-6.0	-60	-148

MSPALU Dynamic Characterization (Prop. Delays)
Typical @ Room Temp. VDD = 10V

Signal Path	Propagation Delay (nsec) typ @ CL = 35pF	
	$T_{P_{LH}}$	$T_{P_{HL}}$
DA or DB ——> DO output, add mode		
Cin = 0	46	62
Cin = 1	55	45
DA ——> DO, pass R	50	74
DB ——> DO, pass S	51	70
DA ——> OVR	61	71
Cin ——> C_{OUT}	29	42
Cin ——> OVR	39	49
Instruction ——> OVR	76	69
Mem Address A ——> DO	78	108
Mem Address B ——> DO	87	104

LOAD=30pf
All times in nsec

TABLE 8
RAYTHEON RB919 PROPAGATION DELAY SUMMARY

	D-Y	S0,S1-Y	S1,S0=LH CLK-Y	S1,S0=LL CLK-Y	(POP) S1,S0=HL CLK-Y
2909 Commercial	17	30	43	43	80
2909 Military	20	40	50	50	90
RB-919*					
+25°C	28.5	35.4	40.9	42.9	69.4
-55°C	25.6	31.8	36.8	38.0	61.6
+125°C	32.16	40.2	46.6	48.1	80.0

	D-CN+4	S0,S1-CN+4	S1,S0=LH CLK-CN+4	S1,S0=LL CLK-CN+4	CN-CN+4
2909 Commercial	30	48	55	55	14
2909 Military	32	50	62	62	16
RB-919*					
+25°C	29.7	36.3	44.3	44.1	17.49
-55°C	27.03	32.7	40.3	39.9	15.77
+125°C	33.3	41.1	49.5	49.3	19.85

*NOTE: RB919 delay values given represent mean values of test results for the total of all chips that passed dynamic testing.

TABLE 9
ROM (RB930) DEVICE CHARACTERIZATION

CMOS/SOS Micro Signal Processor 16K ROM RB-930 Room Temp. (25°C)

Personalization	Serial Number	IDD (MA)	Add → CLK (nsec)	CLK → OUT (nsec)	Word Length (Bits)	Wafer Lot
P22	11	25.9	102	38	8	66C1
	12	33.5	96	40		66C1
	25	1.0	94	42		95C
P23	34	0.1	124	52	16	95D
	32	1.5	130	50		
	31	2.3	130	52		
P24	58	21.7	130	68	32	95A
	61	21.3	130	68		
	60	22.0	116	64		
P25	108	0.1	102	44	32	110F
	110	25.3	98	46		
	114	24.2	94	38		
P26	36	23.0	116	52	16	95B
	38	26.4	114	46		
	40	27.0	122	54		
P27	41	25.4	104	44	8	91B
	50	26.3	96	42		
	47	26.2	94	42		
P28	55	0.2	104	42	8	91A
	57	18.3	86	34		
	51	0.1	118	44		
P29	70	28.2	94	42	8	100A
	69	34.7	84	38		
	74	28.0	90	38		
P30	77	0.2	100	42	16	100B
	80	7.2	104	42		
	79	9.0	100	42		
P31	87	0.1	64	34	32	100C
	92	0.2	74	38		
	91	0.1	78	36		
P32	98	0.1	98	38	8	100D
	106	0.3	106	40		
	99	2.1	82	34		

thresholds and their low temperature performance were improved. The current T^2L compatible input now has a logic zero threshold of 1.3 V and a logic one threshold of 2.2 V. The RB916 was not redesigned to incorporate the new inputs due to schedule requirements.

The other problem, which was not given much weight at the time, was that a small number of the TCS142s shipped to Raytheon from RCA did not pass functional testing. This would be a pattern that continued for the length of the program where devices would fail for no apparent reason. Excessive tristate leakage on the outputs and the device requiring multiple reset pulses to initialize the FIFO mode were also encountered on this device. Because of cost and schedule requirements, no extensive research into these problems was performed, other than keeping track of its failure rate.

It should be noted at this point that the simulations used to generate test vectors on the Sentry VII and VIII testers did not necessarily take into account how the chips were to be used in the Demonstration Processor. The prime case-in-point is the RB917, whose simulation consisted of primarily random inputs exercising the logic without trying to exercise the desired functional requirements. As a result, the RB917 used in the Demonstration Processor did not correctly implement one of its key functions, but this error was not discovered until system testing. (see Subsection 6.2.2.) Mixed-mode simulations of key Demonstration Processor subsections would also have detected the deficiency, but these techniques were not available at the time prior to Demonstration Processor fabrication. The RB918 and RB919 had no such problems.

6.2 System Testing

The purpose of this section is to describe the problems encountered during the checkout of the Demonstration Processor which affected the overall functionality of the design or were unique to CMOS/SOS technology. It will also describe problems associated with the chip set which had not been detected until this point. It should be noted that most of the problems encountered during system testing were simple logic design errors which would have surfaced and been corrected prior to fabrication, had a higher level simulation of the Demonstration Processor been performed. A second source of problems was that the design of the Demonstration Processor was completed before the characterization of the CMOS/SOS arrays. Certain assumptions concerning propagation delays were proved incorrect, and the design of the Demonstration Processor then needed to be modified, where possible, to account for these differences.

6.2.1 DR-11/C Interface Problems

This problem is actually a combination of the low logic thresholds on the RB916 device previously described and also the comparatively slow speeds of the bulk CMOS devices used to implement a large portion of the host computer interface. The primary trouble stems from the fact that when the PDP-11 reads data from the Demonstration Processor, the Data Taken (DTX-1) signal must travel through six levels (worst case) of bulk CMOS gates before actually putting data on the bus to the DR-11/C interface. The delay of approximately 600 nsec associated with this circuitry causes the bus to be read prior to stable data being present on it. The DTX-1 signal was lengthened by changing a capacitor value on the DR-11/C module; however, certain bus ports (CFM, PLO) are still read incorrectly from time to time.

Other I/O problems were encountered by noise on three control signals from the DR-11/C (CSR0, CSR1, DTX) being transmitted through the RB916 buffers, because of the low logic thresholds, resulting in erroneous Demonstration Processor action.

Two of the control signals (CSRO, 1) were cleaned up by passing them through "4000" series device located physically on the Demonstration Processor Test Stand. The DTX signal, which already had too much delay associated with it, could not be so conditioned and had to be left alone. Noise on this signal caused the auto-incrementing counter associated with the Data Memory address to operate erratically, forcing the removal of the counter function.

6.2.2 Pipeline-ADGEN Clock Start-Up

A problem was discovered within the portion of the RB917 R/I chip which serves as the system timing generator for the Pipeline and ADGEN sections of the Demonstration Processor. The problem is a conceptual design error involving enabling and disabling the Pipeline-ADGEN clocks depending on whether the Sequencer FIFO is empty or not. A free-running clock is required to sample the Output Ready signal from the FIFO and start the timing generator, but this signal was not included in the design. The problem has been worked around in the system using spare gates and flip-flops, which allows the Pipeline and ADGEN to start and continue running only if the Sequencer FIFO is never completely emptied. This condition requires dummy Pipeline-ADGEN macro cells to be

added to the program code and hence, increases the execution time of a given routine. The extent of the increase is dependent on the degree of Pipeline-ADGEN utilization within a routine.

6.2.3 Data Memory Write Pulsewidth

A second problem with the system timing generator portion of the RB917 was also found during system test. The problem appears to be a race condition which causes an unwanted transition on the C3 timing signal output. The C3 signal is OR'd with the C2 timing signal to form the write enables used by the Data Memory. The unwanted transition occurs at the time data is changing and could cause erroneous results to be written into memory. The problem is being worked around at present by using only the C2 signal to form the write enables; however, at higher operating frequencies, this signal alone is not wide enough to guarantee correct memory operation.

It should be noted here that the problems described in Sections 6.2.2 and 6.2.3 affect only one RB917 in the Demonstration Processor.

6.2.4 Video Bus (Pipeline Input Bus) Reversal

The 12-bit bus bringing data from data memory to the pipeline, as well as ADGEN and Sequencer, was bit-reversed in two six-bit slices due to a design oversight. An example follows:

Binary	Hex
0001 00 10 0011	123_{16}
0010 00 11 0001	231_{16}

This is only an interconnection problem, but because of the large number of signal points involved, it was decided not to take corrective action.

6.2.5 Sequencer FIFO Shift-In-Shift-Out Timing

During de-bug of the demonstration firmware, it was noticed that data on the output of the Sequencer FIFO was changing, not as a function of Shift-Out (SO) signal as normally expected, but as a function of Shift-In (SI) signal. This problem results from the synchronous implementation of the FIFO memory function in the TCS142 array. In a true FIFO, SI and SO can occur at anytime with respect to each other, since the data being shifted out is held in a register. The TCS142, however, has a transparent latch controlled by the SO signal on its output, so that if data is shifted in while the output latch is transparent (SO high), the input data will appear on the device output, rather than the data due to be shifted out. Once SO goes low, the data is latched and no change takes place until SO goes high again. See Figure 24.

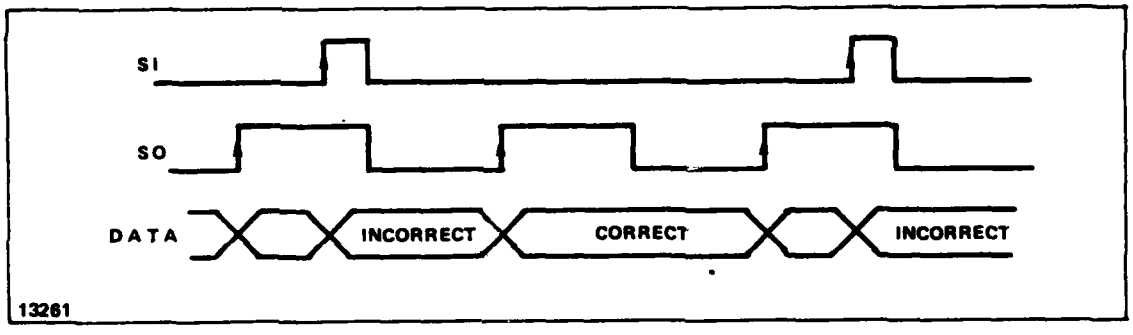


Figure 24 - Original Timing

It was possible to work around this problem, however; although SI (Sequencer clock) and SO (pipeline-ADGEN clock) are supposed to be independent, they are derived from the same raw clock so that a fixed relationship does exist between the two. By shortening the duty cycle of the SO signal, it was possible to obtain a timing arrangement where SI and SO did not conflict. See Figure 25.

Although this problem was solved with no impact on system performance, it should be noted in case this array is used in future designs.

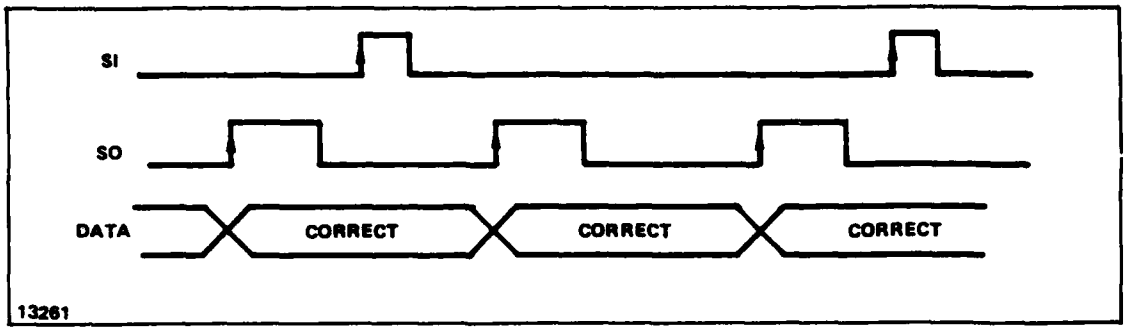


Figure 25 - Revised Timing

6.3 Speed-Power Testing

After determining that all major address and data paths were functional in the Demonstration Processor, an effort was undertaken to determine the maximum operating (microcycle clock rate) speed at 10 V operation. The baseline test used for this was the 256 point FFT which exercises every major block of the pipeline in performing the complex butterfly operation and also gives the ADGEN a workout during the FFT and bit-reverse operations.

The maximum operating speed was determined to be slightly over 2 MHz (less than 2.25 MHz), which is considerably less than the design goal of 6.6 MHz. A combination of several factors is thought to be responsible for these results, and these are detailed below in order of decreasing importance.

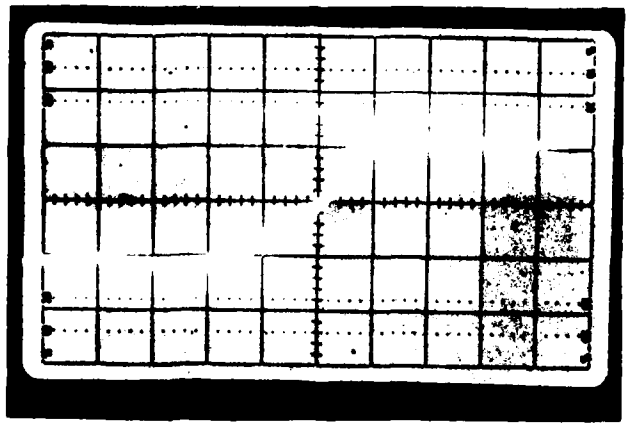
1) Overall System Size and Layout
2) Clock Skew and Distribution
3) Long Delay Paths not accounted for

The major limiting factor, in terms of speed, for CMOS logic is capacitive loading on the system interconnect, which affects the rise and fall times of the signals. This is the result of the high input resistance of CMOS devices; circuit board capacitance can give an RC time constant which will limit system performance. As system speed increase, the value of the RC time constants associated with the system becomes a direct function of the length of the system interconnects and the fanout of each signal. The design rules used for the Demonstration Processor limited the fanout of each output to

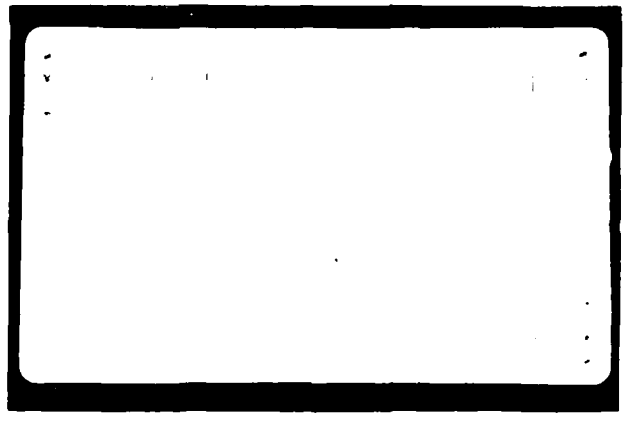
four inputs where possible. The design rules, however, were formulated before the large size printed wiring boards were selected as the packaging medium for the Demonstration Processor. The 11x11 inch boards, plus flex cable, allow signal run lengths of more than 20 inches, which, at an average of 2.5 pF/inch, is 50 pF of capacitive loading not including the input capacitance of the signal destinations. Buffering of the signals would cut down on the capacitive loading, but would introduce additional delay into the logic so that a no-win situation is achieved. Figure 26 shows the effect of capacitive loading on CMOS logic signals.

The most critical of all signals in the Demonstration Processor, in terms of system performance, is the microcycle clock (CL1). In order to comply with the design rule of limiting fanout to four loads, many versions of the basic CL1-1 signal had to be generated. A distribution tree, employing equal levels of gating for all versions, was used, with the design goal being a worst case skew between versions of ten percent of the desired microcycle, 15 nsec. The actual worst case skew was measured to be 70 nsec. This figure was reduced to 40 nsec by the insertion of delays into branches of the tree, although it still does not approach the design goal. The variation of delays is thought to be the result of variations in device parameters, particularly the logic thresholds previously discussed, causing propagation delay variations. A second cause is unequal delays resulting from one signal driving a short run and another driving a long run, thereby giving unequal rise times and causing the destination devices to switch at different points in time. This variation in run length was a result of the use of automatic device placement and routing in the generation of the PWB artwork. A trial system layout had been performed, and a clock distribution scheme placing clock sources as close as possible to destinations was implemented. This layout was then changed around by the PC board placement program, but the clock distribution scheme was not, causing the run lengths to become unequal. A typical clock skew is shown in Figure 27.

Another cause of the reduced system clock speed was the unexpected CLK→Output times of 50 nsec for the R/I (RB917) and ROM (RB930). This is 33 percent of the available time for the design goal clock period expended before any useful function can be performed on the data. The original specification for the R/I called for a CLK→Output of 20 nsec. The additional delay may have extended the length of certain critical paths over the 150 nsec goal.

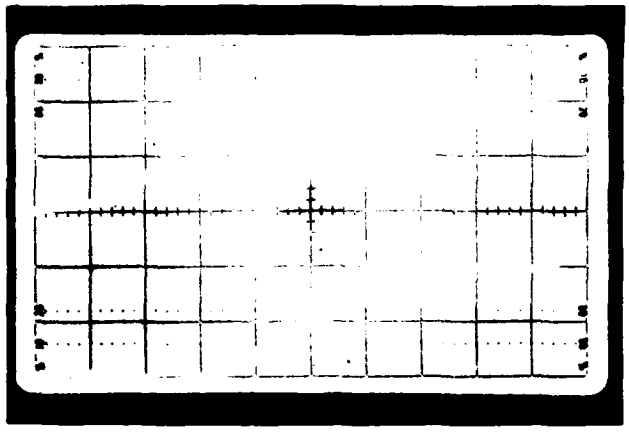


CAR1-1 Signal Driving
1 load over 3 inch run
5 V/cm, 10 nsec/div



VID07-1 Signal Driving
6 loads over 20 inch run

Figure 26 - Effects of Capacitive Loading



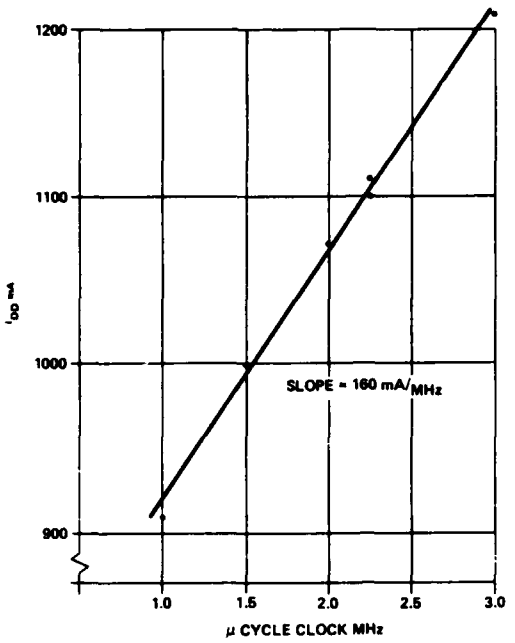
GCL1-1 Top Trace 5 V/cm
LCL1-1 Bottom Trace 5 V/cm
10 nsec/div

Figure 27 - Clock Skew Example

Speed-power measurements were made on the Demonstration Processor and are summarized in Figure 28. If the curve shown is extrapolated out to the design goal of 6.6 MHz, a total power consumption of 33.3 W is obtained. The quiescent power dissipation is due to the level converters and also to device back channel leakage and other processing problems.

6.4 Demonstration Firmware Testing

Five types of firmware algorithms were written for and tested on the Demonstration Processor. These algorithms are described in detail in Volume II of "Computer Software Technical Description". Part of the task of generating these algorithms is writing pipeline microcode which is mask programmed into Read-Only-Memory and thus becomes fixed until new ROMs are fabricated. These microfunctions were simulated on the Verification Processor pipeline simulator prior to committing them to masks, but differences between the two machines due to the architectural enhancements described in Section 4 allowed some functions not be confirmed. Sixteen pipeline macros were coded and put into ROM, and two of these macros were found to have errors. Overall testing of



CL1-1 RATE (MHz)	I_{DD}-10 V(mA)	I_{CC}-5 V (A)
IDLE	780	3.0
1.0	910	3.0
1.5	1000	3.0
2.0	1070	3.0
2.25	1100	3.0
2.50	1140	3.0
2.75	1165	3.0
3.0	1200	3.0

Figure 28 - Speed-Power Data

the firmware on the Verification Processor did not start until after fabrication of the ROMs had started, and at this point it was discovered that two additional pipeline macro functions were needed for proper firmware operation.

Only two of the algorithms were affected by these errors and omissions: the CFAR detection routine and the Coordinate Conversion routine. The details are:

CFAR Detection Routine

1) Sliding Window Sum (SWS) micro in error. Running sum not being held in pipeline holding register after adding the difference between the new point and the point being dropped.
2) Threshold, Link, Count (THC) micro in error. Wrong pipeline flag condition selected to test if data exceeds threshold.
3) Pack (PAC) micro omitted.

Coordinate Conversion Routine

1) Vector Add (VAD) micro omitted.

7. RECOMMENDED CORRECTIVE ACTIONS

The Demonstration Processor achitecture has shown itself to be flexible and suitable to a wide variety of avionics and guidance applications. The CMOS/SOS chip set used to implement the Demonstration Processor has the potential to perform at the desired speeds given the proper packaging concept and the following design modifications:

1) Modification of R/I (RB917) to correct problems noted in Sections 6.2.2 and 6.2.3.
2) Correction of ROM contents to correct firmware deficiencies.
3) Packaging system in smaller modules and having necessary clock signals regenerated on each module synchronized from a common master clock. This should alleviate clock skew and clock loading problems.

APPENDIX A

REGISTER/INTERFACE CHIP (RB917) DEVICE SPECIFICATION AND BONDING DIAGRAMS

1.0 Introduction

The Register/Interface (RB917) chip is an integral element within the Micro Signal Procesor as shown in Figure A-1. The Micro Signal Processor is being developed as a Technology Program with AFAL under contract F33-615-77-C-1224. This array provides T^2L to CMOS and CMOS to T^2L conversion as well as general purpose multiplexing and registers in 8 bit slices. Since many of the data paths within the Micro Signal Processor are 12 bits, the RB917 can be placed in a smaller 48 pin hermetic chip carrier and be bonded to function as a 6 bit wide slice. This results in considerable space saving in the final form factor.

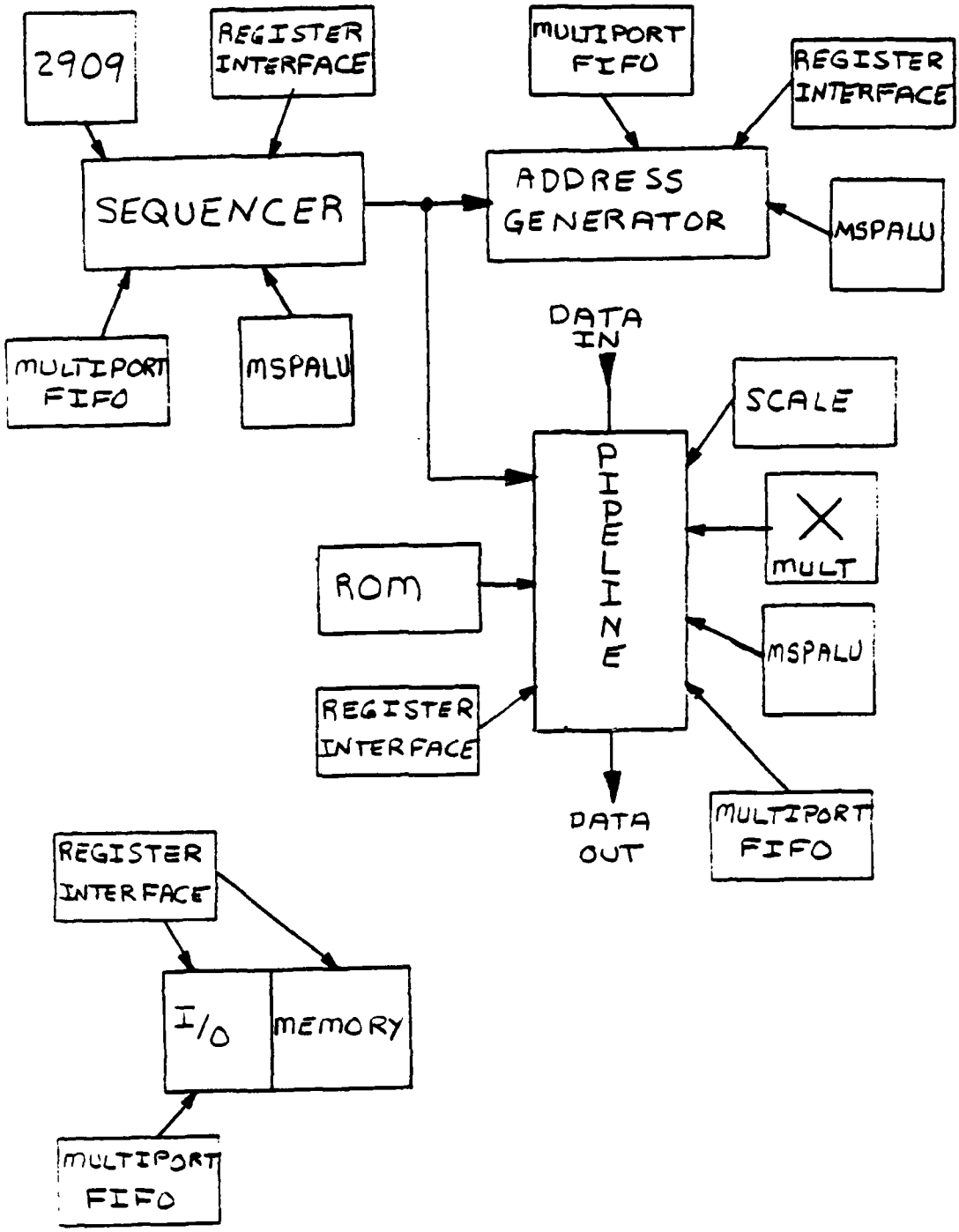


Figure A-1 CMOS/SOS Chip Allocation

2.0 Device Definition

The Register/Interface chip is used throughout the Micro Signal Processor to provide a variety of required functions. These functions are listed according to module location in the μSP as follows:

I. Sequencer - a. T^2L to CMOS Level Conversion
b. CMOS to T^2L Level Conversion
c. Multiplexer/Register for Address Inputs to Sequencer Memory

II. ADDRESS GENERATOR - a. T^2L to CMOS Level Conversion
b. CMOS to T^2L Level Conversion

III. I/O - a. Timing circuitry

IV. Coefficient Memory - a. Address Multiplexer Register
b. Output Register
c. CMOS/T^2L Level Conversion
d. T^2L to CMOS Level Conversion

V. Data Memory - a. T^2L to CMOS Level Conversion
b. CMOS to T^2L Level Conversion
c. Multiplexer for Address
d. Registers for Data Interface to Arithmetic Pipeline and video bus
e. Auto Increment Counter

VI. Pipeline - a. Instruction Decode
b. Registers for Micro Delay
c. CMOS to T^2L Level Conversion for PROM's
d. T^2L to CMOS Level Conversion

These functions are detailed in Section 2.1.

2.1 Functional Definition

The Register/Interface array performs several functions in the Micro Signal Processor. The functions, which will be described in detail in this section, include the following:

a. Register storage
b. Multiplexing
c. CMOS/SOS to T^2L level conversion
d. T^2L to CMOS/SOS level conversion
e. Coefficient memory segmentation mask logic (8-bit version only)
f. Data Memory Auto-increment counter (8-bit version only)
g. SSI gates for decoding, etc.
h. System clock generation (8-bit version only)

The requirement for level conversion occurs frequently in the µSP because of use of T^2L memory (RAM). Today's technology requires using memories whith are not 10V SOS compatable. Most inputs on this chip (marked with an asterisk,*, in Section 2.2) must accept T^2L level inputs with the chip operated at 10V. Several outputs have separate output power pins to allow T^2L level outputs while the SOS chip operates at 10V.

Figure A-2 shows the functional block diagram of the entire array. Note that several inputs and outputs have common pins. The tri-state enables determine which function a given chip performs. The Registers and Multiplexer have individual tri-states and output voltage (power) pins. The first 8-bit register serves as an 8-bit general purpose counter. This will provide auto increment for data memory. The mask logic performs a 3 line to 8 decode where all lower order bits (below the one selected) are logic zero as well as the selected bit.

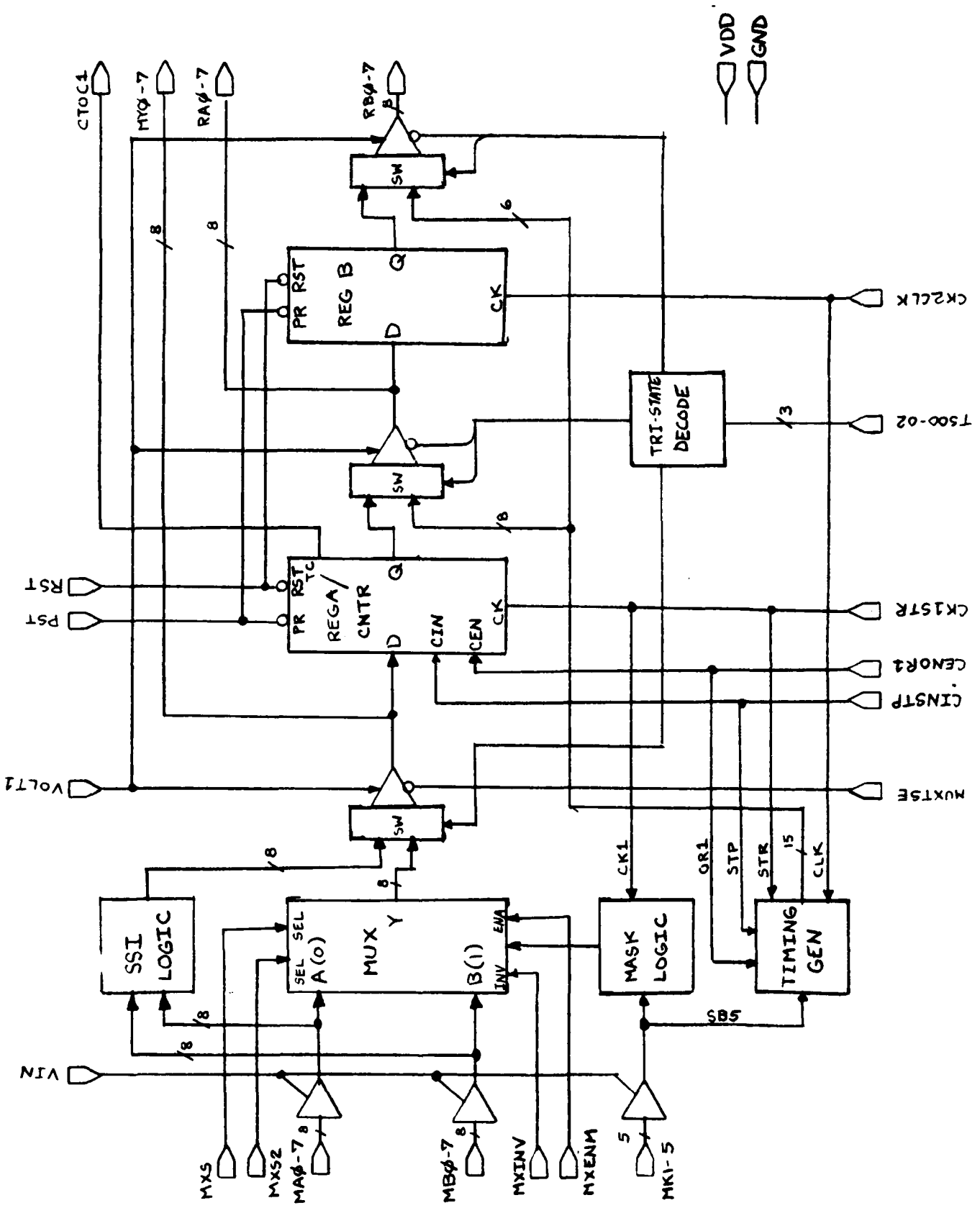


Figure A-2 RB917 Block Diagram

The SSI gates are shown in Figure A-4. These gates provide the logic required in various areas, such as pipeline micro instruction repeat/decode. These gates also provide a 'safety factor' to allow for potential minor design changes or flaws.

The timing circuitry provides most of the system clocks, as well as single step control. The waveforms generated are shown in Figure A-3. This timing diagram assumes start up from a halt condition.

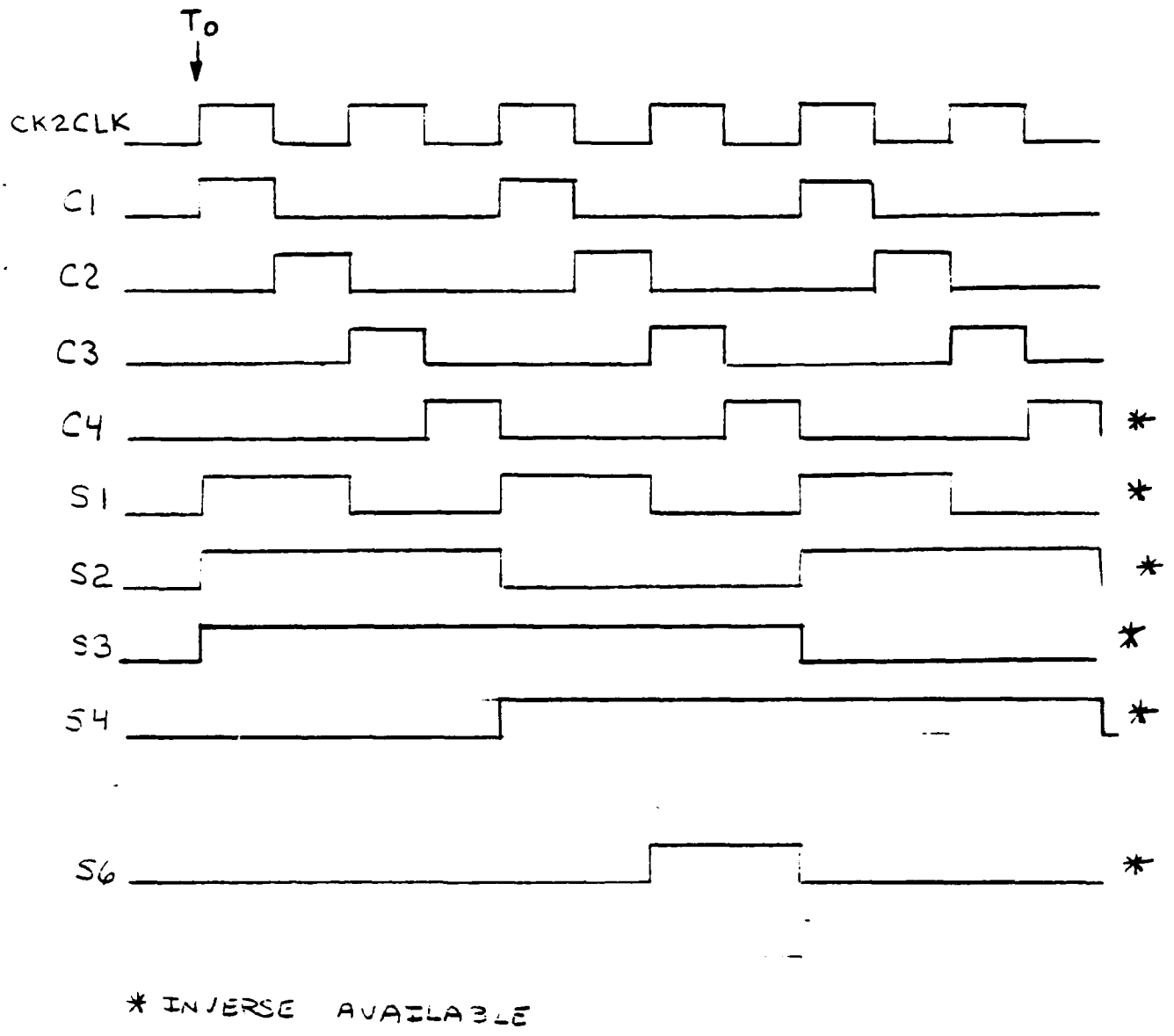


Figure A-3 Waveforms CMOS/SOS μSP Timing Generator

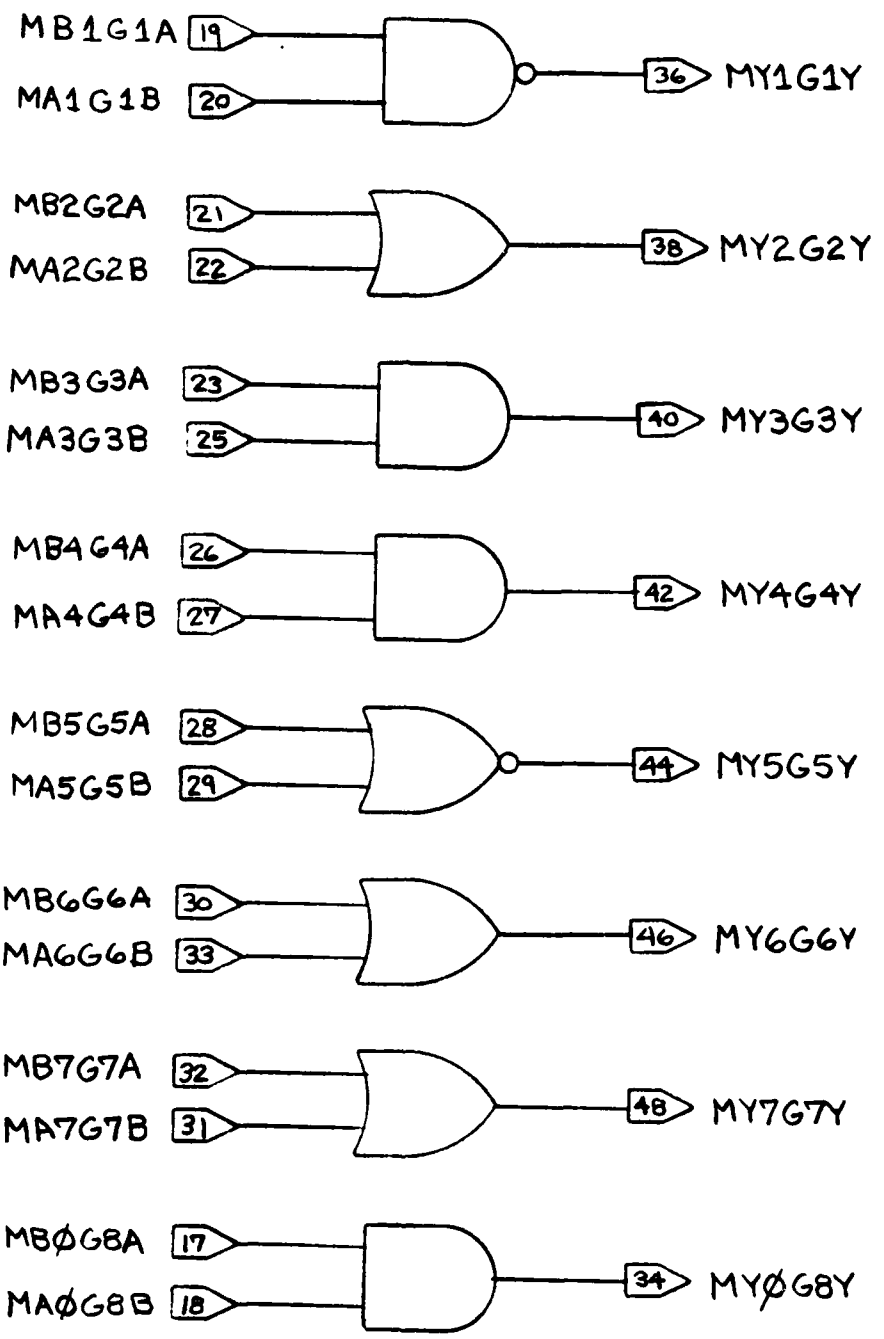


Figure A-4 RB917 SSI Logic

2.2 Input Definition

The following is a list of inputs to the Register/Interface Chip. Where a pin serves more than one function, the individual functions are separately described.

Signals marked with an asterisk,*, are T^2L compatible, controlled by the VIN signal, pin 64. Those signals marked with a delta, Δ, should be designed for minimum delay in order to optimize μSP performance.

PIN	SIGNAL	FUNCTION(S)
18	MA0G8B*	a. Multiplexer A input LSB (Bit 0) b. Input 2 to Gate 8
20	MA1G1B*	a. Multiplexer A input Bit 1 b. Input 2 to Gate 1
22	MA2G2B*	a. Multiplexer A input Bit 2 b. Input 2 to Gate 2
25	MA3G3B*	a. Multiplexer A input Bit 3 b. Input 2 to Gate 3
27	MA4G4B*	a. Multiplexer A input Bit 4 b. Input 2 to Gate 4
29	MA5G5B*	a. Multiplexer A input Bit 5 b. Input 2 to Gate 5
33	MA6G6B*	a. Multiplexer A input Bit 6 b. Input 2 to Gate 6
31	MA7G7B*	a. Multiplexer A input MSB (Bit 7) b. Input 2 to Gate 7
17	MB0G8A*	a. Multiplexer B input LSB (Bit 0) b. Input 1 to Gate 8
19	MB1G1A*	a. Multiplexer B input Bit 1 b. Input 1 to Gate 1
21	MB2G2A*	a. Multiplexer B input Bit 2 b. Input 1 to Gate 2
23	MB3G3A*	a. Multiplexer B input Bit 3 b. Input 1 to Gate 3

26	MB4G4A*	a. Multiplexer B input Bit 4 b. Input 1 to Gate 4
28	MB5G5A*	a. Multiplexer B input Bit 5 b. Input 1 to Gate 5
30	MB6G6A*	a. Multiplexer B input Bit 6 b. Input 1 to Gate 6
32	MB7G7A*	a. Multiplexer B input MSB (Bit 7) b. Input 1 to Gate 7
43	CK1STR	a. Clock to 8-bit register A (Δ) b. Start command to timing logic
45	CK2CLK	a. Clock to 8-bit register B (Δ) b. High speed input clock to timing logic (Δ)
60	VOLT1	Output driver voltage for MY, RA, RB outputs.
64	VIN	Input voltage control for MA, MB, MK inputs.
14	TS00	Tri-state select for SSI logic;
13	TS01	Register A
12	TS02	Register B and Timing

TS00 TS01 TS02	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
REGISTER A →	E	E	Z	Z	Z	Z	Z	E
REGISTER B →	Z	E	E	Z	Z	Z	E	E
SSI	Z	Z	Z	Z	Z	E	E	E
TIMING	Z	Z	Z	Z	E	Z	Z	Z

Z = HIGH Z STATE

E = ENABLED

10	MUXTSE	Tri-state enable for Multiplexer Output pins 44-51. Logic 0 = enable, logic 1 = high Z
9	CENOR1	a. Count enable to register A which when logic one, disables register inputs and allows register to act as an 8 bit counter. b. OR1 signal to timing logic
11	CINSTP	a. Carry in to counter. When CENOR1 is logic 1, this signal acts to allow counting for multistage counters. b. STP signal to timing logic
34,36,38,40, 42,44,46,48 See Note 1		Inputs to Register A if multiplexer tri-state is disabled. These pins are used as outputs as described in Section 2.3.
49,51,53,55, 58,61, 2,63 See Note 1		Inputs to Register B if Register A tri-states are disabled. These pins are used as outputs as described in Section 2.3.
37	MK1*	a. Control bit to mask logic. This bit enables the masking process when logic 1 and MK2 is also logic 1.
39	MK2*	a. Control bit to mask logic. This bit forces multiplexer select line to logic 1. (B inputs.)
41	MK3*	a. Input to mask logic. This bit is MSB of 3 bit code (pins 54-56) which determine level of masking as shown in the table .

7	MK4*	a. Second bit to mask logic priority encode (see table).
4	MK5SB5*	a. LSB of 3-bit code to mask logic. If MK1 is logic 1 and MK2 is also logic 1 the multiplexer select lines are forced to logic 0 for all bits equal to the binary code plus 1 as shown in the table. The select lines are held following the next clock (CK1STR) until MK2 = logic 1 with MK1 = logic 0.
		b. Bus control bit to timing logic, logic 1 allows free run, logic 0 allows single single operation.

MK3	MK4	MK5SB5	MK1	MUX Select Lines Forced to Logic 0
X	X	X	0	None
0	0	0	1	1 (MSB Only)
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8 (all)

6	MXS	a. Multiplexer high order select line 0 = MA (4-7) inputs, 1 = MB (4-7) input pins.
35	MXS2	MUX selects for low order, 0 = MA (0-3), 1 = MB (0-3).
56	VDD	+10V
24	GND	Return
47	MXENM	Multiplexer/Segmentation select, logic 1 enables segmentation mask control of multiplexer. Logic 0 allows Pins 6 and 35, MXS and MXS2, to control multiplexer.
5	MXINV	Logic 1 inverts output of multiplexer.
16	RST	Reset to registers (active low)
15	PST	a. Preset all registers to logic 1 (active low)

NOTE: 1. These pins can serve as either outputs or inputs, depending on tri-state selection. These pins are listed here and detailed in Section 2.3 as output functions.

2.3 Output Definition

The following is a list of outputs from the Register/Interface chip. The list is by chip pin numbers. Where a pin serves as output for 2 functions, both are defined, along with the state of the tri-state enable which enables each output function. In the case of the Multiplexer and Register A outputs, these pins may be used as inputs to the Register A and Register B respectively. This requires the output tri-state be turned off. For example: If MUXTSE pin 50 is logic 1, pins may be used as external inputs to Register A.

Those signals marked with an asterisk, (*), must be T^2L compatible at 10V operation. All output voltages are controlled by the COLT1 signal, pin 60. Those signals marked with a delta, (Δ), should be designed for minimum delay to optimize μSP performance.

PIN	SIGNAL	DESCRIPTION
8	CTOC1	a. Counter carry out (terminal count) b. Clock C1 output
34	MY0G8Y*	a. Bit 0 (LSB) out of Multiplexer b. Output of Gate 8
	NOTE:	If tri-state for Multiplexer and SSI logic is disabled, then Pin 34 is LSB input to Register A.
36	MY1G1Y*	a. Bit 1 out of Multiplexer b. Output of Gate 1
38	MY2G2Y*	a. Bit 2 out of Multiplexer b. Output of Gate 2

40	MY3G3Y*	a. Bit 3 out of Multiplexer b. Output of Gate 3 See Pin 34
42	MY4G4Y*	a. Bit 4 out of Multiplexer b. Output of Gate 4
44	MY5G5Y*	a. Bit 5 out of Multiplexer b. Output of Gate 5
46	MY6G6Y*	a. Bit 6 out of Multiplexer b. Output of Gate 6
48	MY7G7Y*	a. Bit 7 (MSB) out of Multiplexer b. Output of Gate 7
49	RA0C2*	a. Bit 0 (LSB) out of Register A b. Clock C2 from timing logic
	NOTE:	If tri-states for both Register A and timing are in the high impedance state then the "RA" pins can be used as inputs to Register B (LSB-MSB).
51	RA1C3*	a. Bit 1 out of Register A b. Clock C3 from timing logic
53	RA2C4*	a. Bit 2 out of Register A b. Clock C4 from timing logic
55	RA3C4N*	a. Bit 3 out of Register A b. Clock C4N from timing logic
58	RA4S1N*	a. Bit 4 out of Register A b. Clock S1N from timing logic
61	RA5S1*	a. Bit 5 out of Register A b. Clock S1 from timing logic
2	RA6S2*	a. Bit 6 out of Register A b. Clock S2 from timing logic
63	RA7S2N*	a. Bit 7 (MSB) out of Register A b. Clock S2N from timing logic

50	RB0S3*	a. Bit 0 (LSB) out of Register B b. Clock S3 from timing logic
52	RB1S4*	a. Bit 1 out of Register B b. Clock S4 from timing logic
54	RB2S 3N*	a. Bit 2 out of Register B b. Clock from timing logic S3N
57	RB3S6*	a. Bit 3 out of Register B b. Clock S6 from timing logic
59	RB4S6N*	a. Bit 4 out of Register B b. Clock S6N from timing logic
3	RB5S4N*	a. Bit 5 out of Register B b. Clock from timing logic S4N
1	RB6*	Bit 6 of Register B
62	RB7*	Bit 7 (MSB) out of Register B

TOTAL PINS 64

Figures A5 through A7 are logic diagrams and Figures A8 and A9 are bonding diagrams.

TABLE A-1

DEVICE SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	$-55^{\circ}C$ to $+125^{\circ}C$
Non-operating	$-65^{\circ}C$ to $+150^{\circ}C$
Supply Voltage	+15V non-operating
Input Voltage	-.5V to Vcc +.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	-	250	µamp
VOL Output Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input Low	5 10	-	-	1.5 3.0	Volts
VIH Input High	5 10	3.5 7.0	-	-	Volts
IO Outputs Sink and Source	5 10	-	1.5 (within .5V of Supply or GND 1.5		ma
Iin Input Current	0<Ein<Vcc	-	.3	.1	µamp
Cin data/clock	any	-	2	3/5	pf
Vcc	-	4.5	10	12	Volts

NOTES: 1. Iin for $T^2L \approx 200\mu A$

2. Vin for T^2L - Logic >2.0V
<0.8V

TABLE A-2

SWITCHING CHARACTERISTICS GENERAL

CHARACTERISTICS	Vcc	MIN	TYP	MAX	UNITS
OUTPUT RISE AND FALL TIME (15pf load)	5 10	-	30 15	40 18	nsec nsec
DATA SETUP TIME (REGISTERS)	10	-	5	7	nsec
DATA HOLD TIME (REGISTERS)	10	-	8	10	nsec
CLOCK WIDTH (REGISTERS)	any	50	75	-	nsec
CLOCK RATE	5 10	 6.66	3.0 6.66	-	MHZ MHZ
CLOCK TO OUTPUT (REGISTER)	10	-	15	20	nsec
PD @6.6 MHZ	10	-	-	300	mW

PACKAGING

64 pin leadless carrier .72 X .72 KOYTO or equivalent

48 pin leadless carrier .56 X .56 KOYTO or equivalent

NOTE: 10 volt specifications shall take precedence in design criteria. The 5V specifications are guidelines.

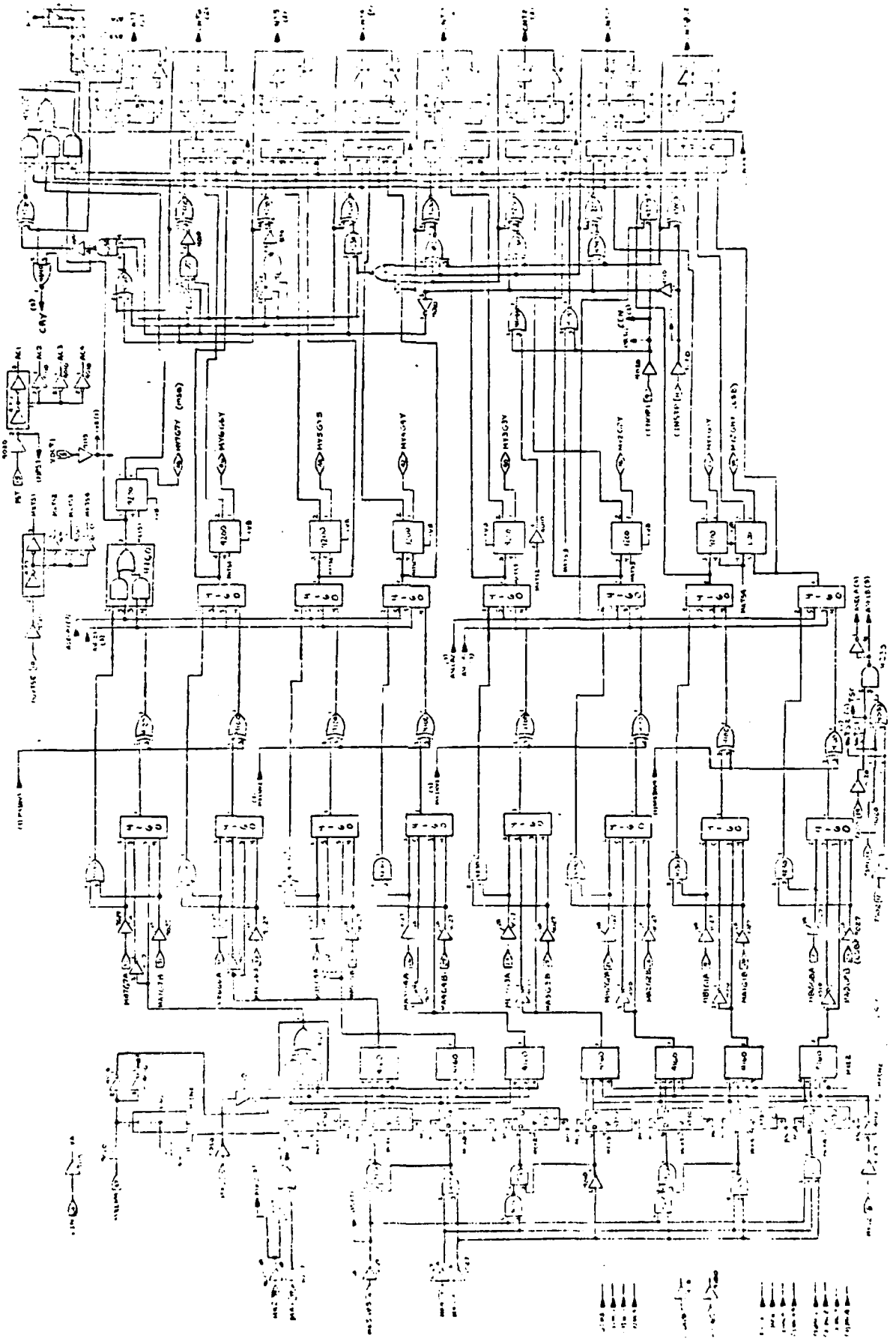


Figure A-5 Register/Interface Chip MUX/SSI/RB917/MASK LOGIC/COUNTER

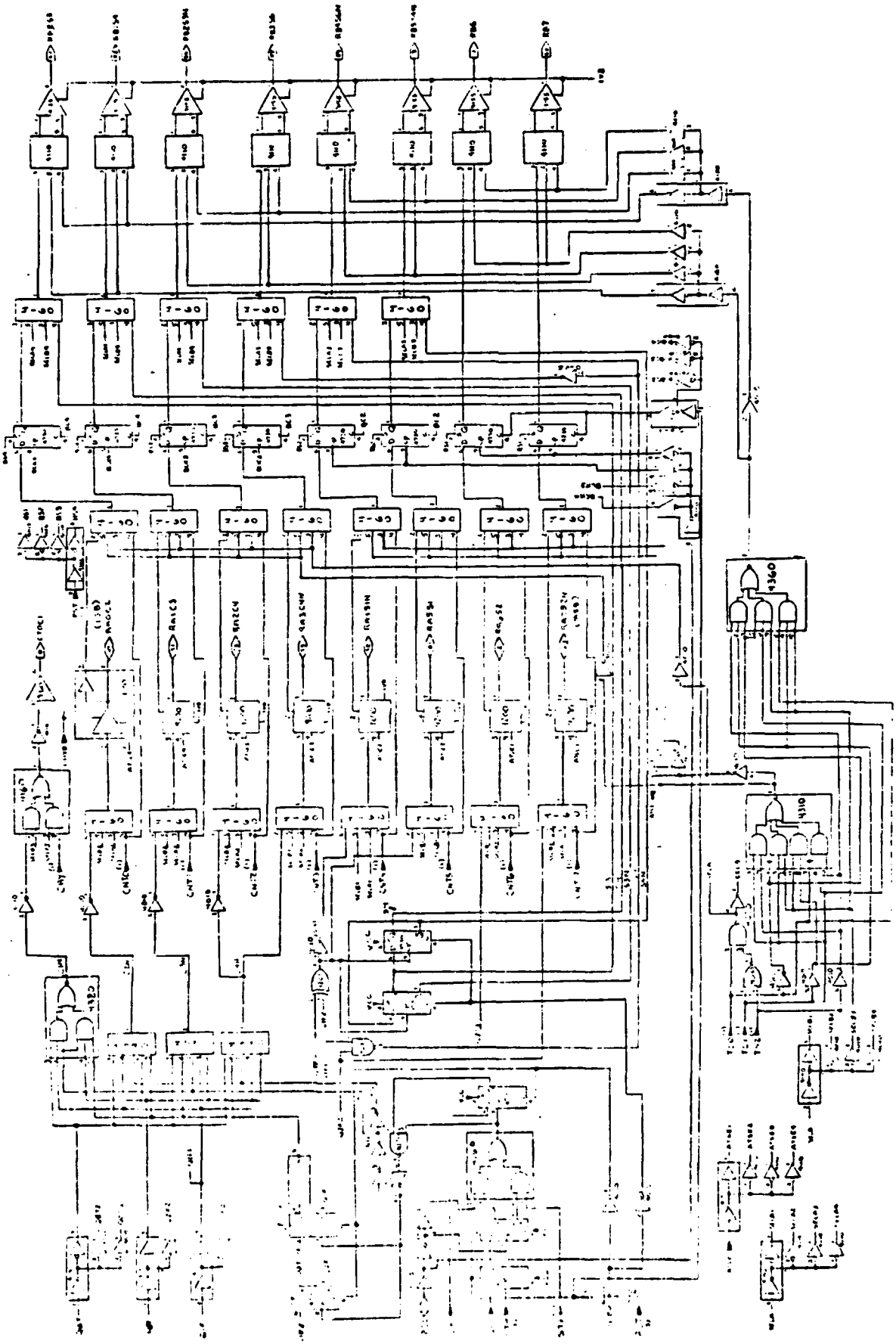


Figure A-6 Register Interface Chip Timing/Reg B/Tri-State Decode

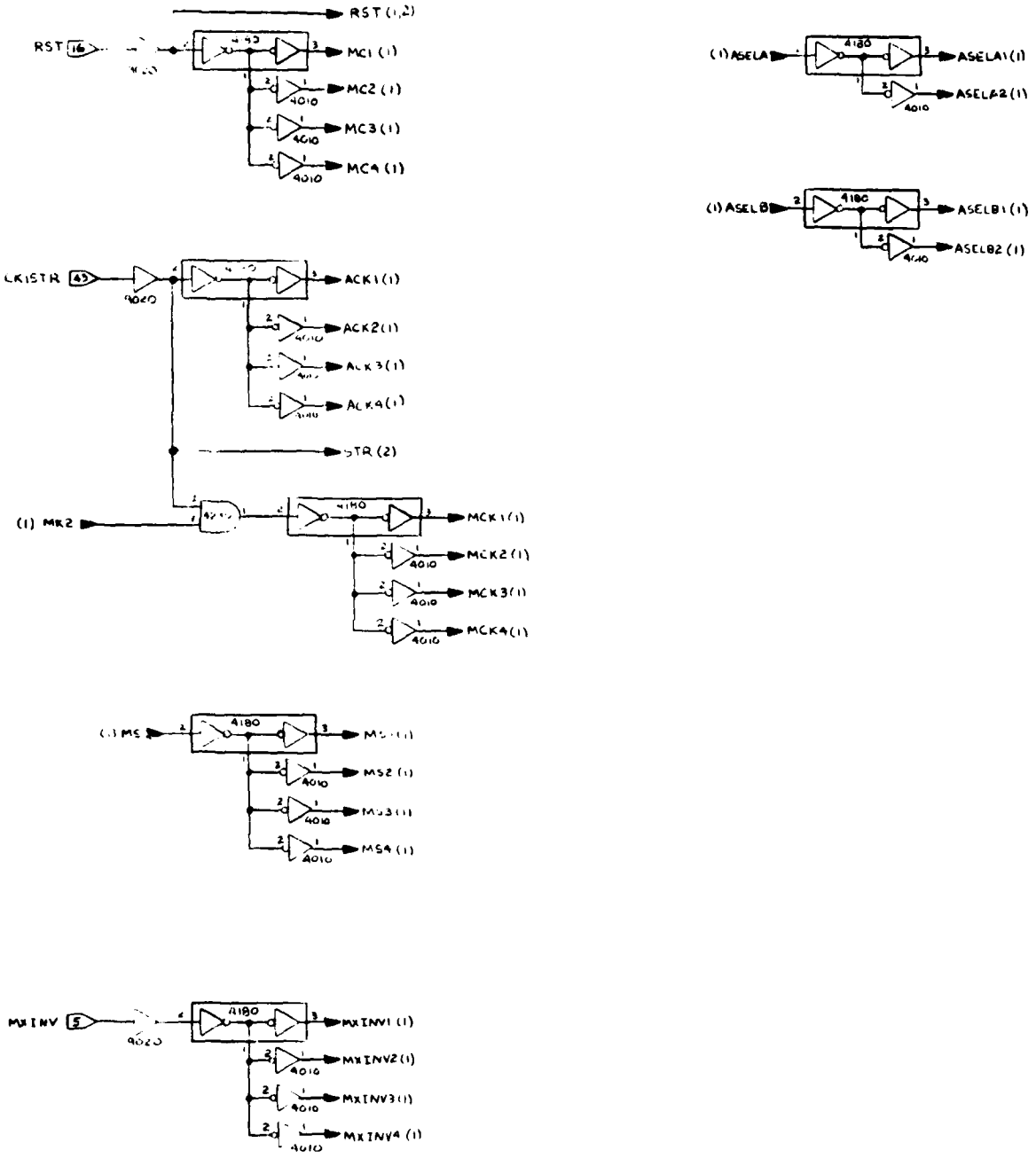


Figure A-7 Register/Interface RB917

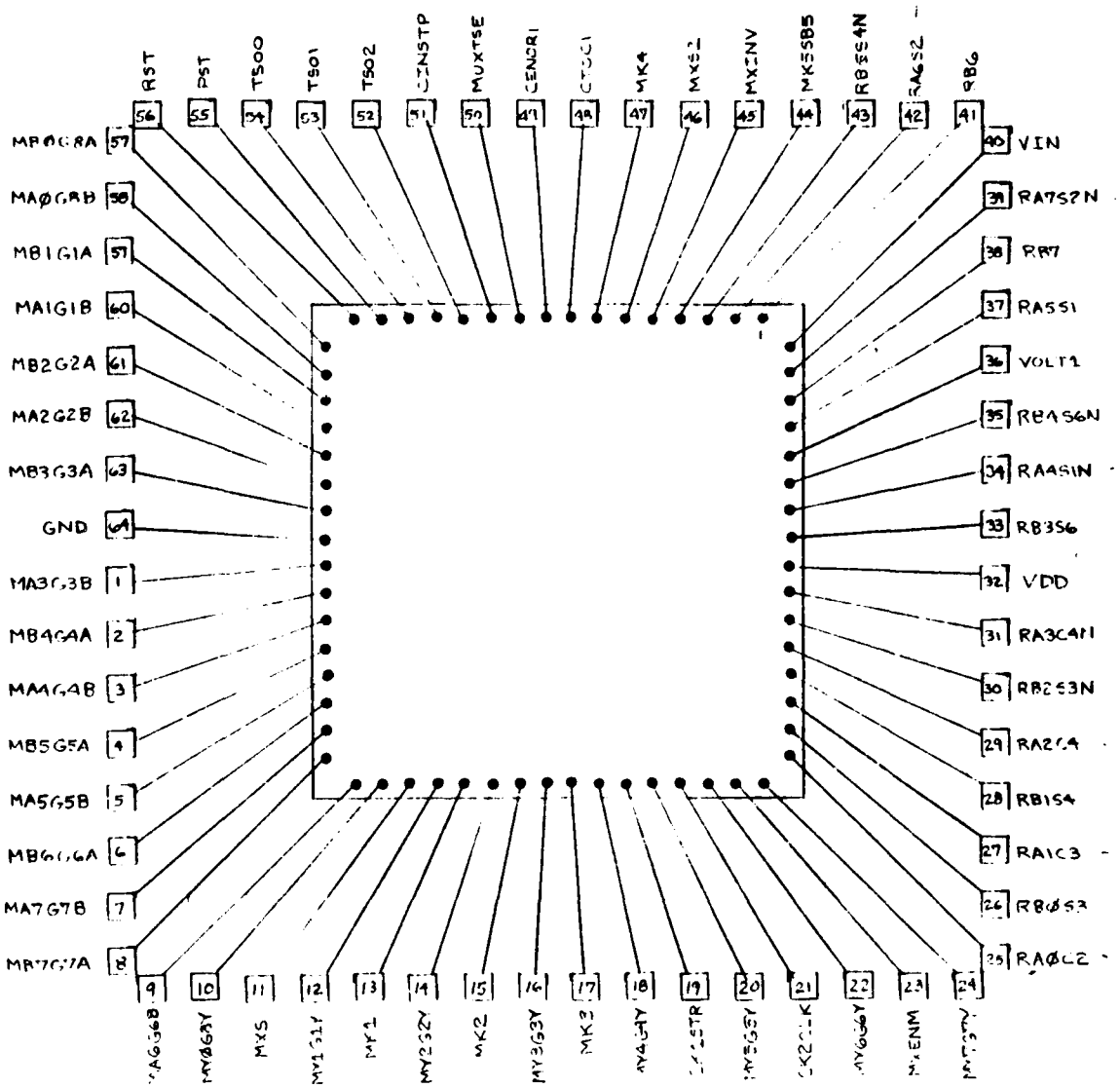


Figure A-8 RB917-64 (R/I) Bonding

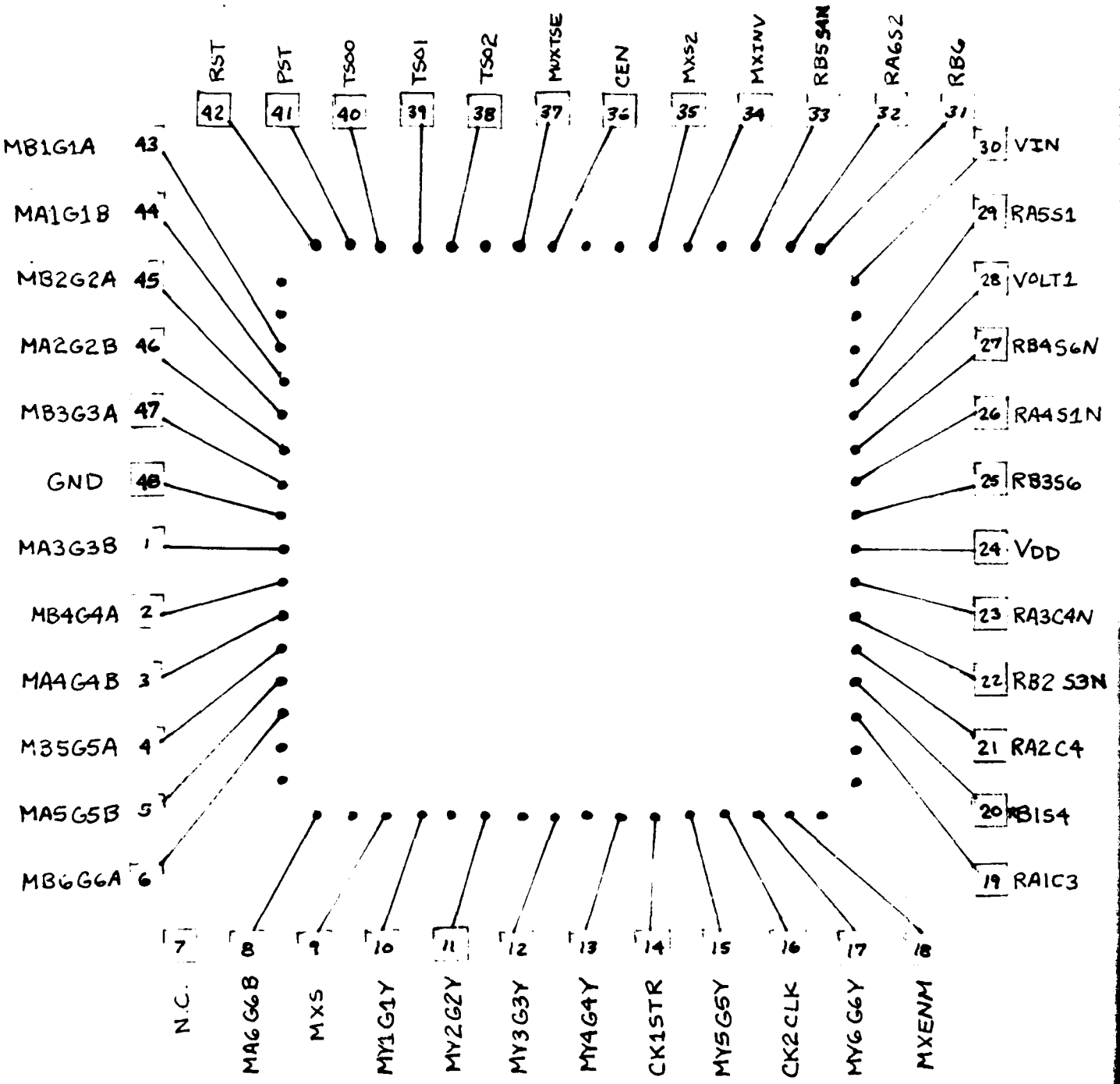


Figure A-9 RB917-48 Bonding

APPENDIX B

MSPALU DEVICE DESCRIPTION AND SPECIFICATION

1.0 GENERAL DESCRIPTION

The RB-918 MSPALU is an 8-bit wide cascadable arithmetic logic unit with full carry-lookahead across all eight bits. As shown in the block diagram this device includes a 16-word by 8-bit multiport RAM, an 8-bit high speed ALU, and associated multiplexers. A 4-bit op-code selects one of 10 ALU functions and 3 more bits are used for memory and ALU source selection. The multiport memory has 3 distinct address busses: 2 read addresses (A and B) and 1 write address (W). The ALU output is bussed to the memory input MUX to allow results to be written back to the multiport memory after an operation.

1.1 Architecture

A block diagram of the RB-918 MSPALU is shown in Figure B-4. The circuit is an 8-bit slice cascadable to any number of bits. All data paths within the device are 8-bits wide. The 2 key elements of the MSPALU are the 16-word by 8-bit multiport memory and the 3-bit high speed ALU.

The 16-word multiport memory has 3 distinct ports and address busses. When the write enable signal ($\overline{WE}$) is low, data is always written into the multiport RAM, at the location indicated by the write address bus (WØ-W3). This input data can come from 1 of 2 sources as selected by I2. When I2 is low, the ALU output is enabled to the memory. When I2 is high, external data (BPØ-BP7) is selected. Data is read from the memory through the YA and YB outputs. The A address bus (AØ-A3) selects the location whose contents will appear at the A-port (YAØ-YA7), and the B address bus does the same for the B-port.

The memory outputs drive separate 8-bit latches. These latches hold RAM output data while the clock input (CP) is low, and pass data when the clock is high. This eliminates any possible race conditions that could occur when new data is being written into the RAM. Connecting $\overline{WE}$ and CP together allows control of the memory and latches with one signal, if data is written every cycle.

The high speed arithmetic logic unit (ALU) can perform 3 arithmetic and 7 logical operations on the 2 8-bit input words, R and S. The R input can be selected from either the A-port of the memory if I∅ is low, or external data (DA∅-DA7) if I∅ is high. The S-input operates similarly, utilizing the B-port and DB∅-DB7, and I1 for selection. A status bit is also developed from the logical "OR" of the S inputs to the ALU. This signal (ABD) can be used to detect all zeros on the S input.

The ALU operation that will be performed is selected by the 4-bits I3, I4, I5 and I6. The operations as defined by these bits are shown in Table B-1. The block diagram shows no generate ($\overline{G}$) or propagate ($\overline{P}$) outputs, but rather only a CN8 "ripple carry" output. This is because the 64-pin leadless-carrier package does not allow for all of these outputs (ref. memo #7676-79-741). However, as is indicated in the referenced memo, with only 2 slices being cascaded, since the CN8 output is actually a fast carry, the $\overline{G}$ and $\overline{P}$ outputs are not needed. These signals are still produced within the chip and do come out to pads, but these pads will not be bonded to pins on the leadless carrier. A future application may utilize these signals.

The CN input is the carry-in to the ALU. An additional input, PERCN, is used to "personalize" the chip. When PERCN is set to a 1, a carry-in will be forced during a subtract operation. This allows for automatic 2's complement arithmetic. In a system with more than 1 slice cascaded, only the least significant slice would have PERCN set high.

The ALU also has 3 other status outputs. The F7 output is the most significant (sign) bit of the ALU. F7 is non-inverted with respect to the D∅7 output. The FE∅ output is used for zero-detect in the ALU output. FE∅ is high when all F outputs are low. The overflow (OVR) output indicates a 2's complement overflow into the sign bit, i.e. when CN7 and CN8 are not the same polarity. This signal is simply an exclusive OR of CN7 and CN8.

TABLE B-1
ALU FUNCTION CONTROL

Function

I_6	I_5	I_4	I_3	OCTAL CODE	FUNCTION	SYMBOL
L	L	L	L	0	R Plus S	R + S
L	L	L	H	1	S Minus R	S - R
L	L	H	L	2	R Minus S	R - S
L	L	H	H	3	R Or S	R ∨ S
L	H	L	L	4	R And S	R ∧ S
L	H	L	H	5	R XOR S	R ∀ S
L	H	H	L	6	R	R
L	H	H	H	7	S	S
H	L	L	L	10	R Plus S	R + S
H	L	L	H	11	S Minus R	S - R
H	L	H	L	12	R Minus S	R - S
H	L	H	H	13	R Or S	R ∨ S
H	H	L	L	14	R And S	R ∧ S
H	H	L	H	15	$\overline{R}$ And S	R ∧ S
H	H	H	L	16	R	R
H	H	H	H	17	R XNOR S	$\overline{R \forall S}$

CN — Carry in to ALU (see 2901A).

BP0-3P7 — Direct data in to multiport. 3P0 is the LS3.

I2* — Control bit for multiport input multiplexer. Logic 0 selects ALU data to the multiport. Logic 1 selects external inputs.

TSE — Tri-state enable. Logic 0 = enable outputs, Logic 1 = high Z state.

PERCN — Carry-in personalization control. Logic 0 allows normal ALU operation. Logic 1 forces a logical carry-in to the ALU for the subtract operation.

TOTAL INPUT PINS = 48

The ALU output is passed back to the multiport data input as well as being passed to a tri-state buffer. The tri-state enable signal (TSE) will enable the outputs when low and put the ALU outputs into the high impedance state when high. TSE has no effect on any status outputs or the carry output.

1.2 Logic Implementation

The BB-918 MSPALU utilizes fast lookahead-carry for its arithmetic operations. This is best visualized as a 2-step binary addition process. The first step involves doing a bitwise "half-add". In other words, each pair of bits is added without preserving any carry that may occur. While this is happening, all carries are being generated via the carry-lookahead process. The second step adds the half-sum to the carries in another bitwise half-add, to produce the final result. The lookahead logic allows all carry bits to be generated at nearly the same time, and consequently the full sum can occur in close to the time it would take for a single bit.

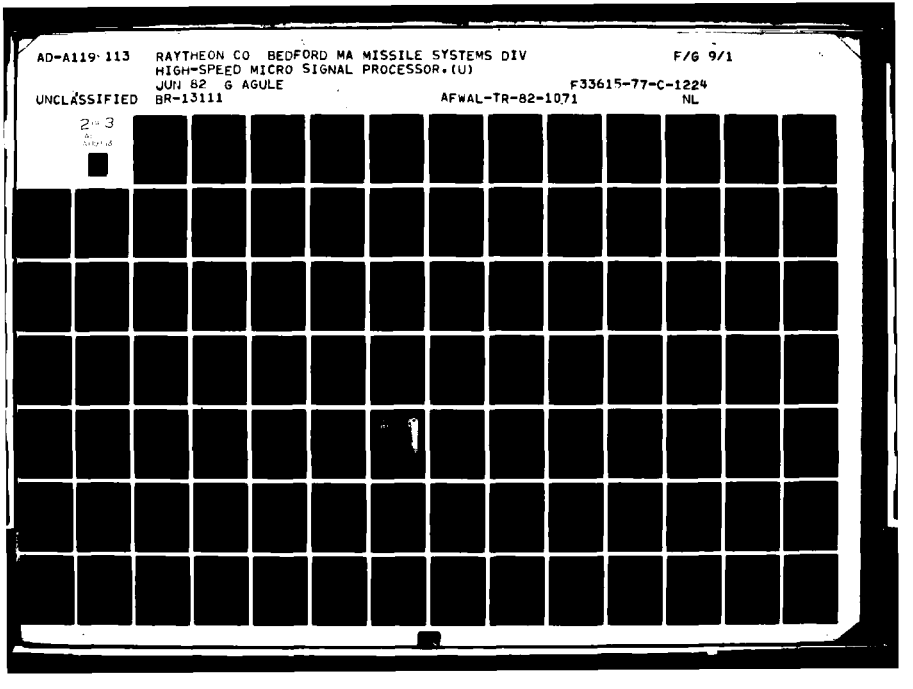
To produce the various arithmetic and logical functions in the ALU, a generalized logic function type is used. This general function has the form $\overline{R_L S_L + R_R S_R}$ where R_L,S_L,R_R and S_R can each be inverted or not, and the NOR function can also be an OR. Fig. B-5 shows the basic logic element used for each bit in the ALU. Table B-2 shows the ALU function, op-code, and equivalent function used to implement each operation.

There are basically, 7 control signals that define what ALU operation occurs. These 7 signals (RL,SL,RR,SR,CIN,CE and CS) must be mapped from the 4 instruction bits, I_3, I_4, I_5 and I_6. RL,SL,RR and SR determine whether each of the 4 inputs to the logic element is true or inverted. CIN, CE and CS manipulate the carry bits. CIN sets the carry-in to bit zero during a subtract if PERCN is high. CE disables all carries generated by the lookahead logic when high to allow logical

TABLE B-2

OPERATION FUNCTIONS

ALU FUNCTION	EQUIVALENT FUNCTION	OP-CODE A I_6	B I_5	C I_4	D I_3	RL	SL	RR	SR	CIN	CE	CS
R Plus S	$\overline{R\bar{S}} + RS$	0	0	0	0	0	0	1	1	0	1	0
S Minus R	$R\bar{S} + \bar{R}S$	0	0	0	1	1	0	0	1	1	1	0
R Minus S	$\bar{R}S + R\bar{S}$	0	0	1	0	0	1	1	0	1	1	0
R Or S	$\bar{R}\bar{S} + \bar{R}\bar{S}$	0	0	1	1	0	0	0	0	X	0	X
R And S	$RS + RS$	0	1	0	0	1	1	1	1	X	1	1
R XOR S	$\overline{R\bar{S}} + RS$	0	1	0	1	0	0	1	1	X	0	X
R	$\bar{R}S + \bar{R}\bar{S}$	0	1	1	0	0	1	0	0	X	0	X
S	$\bar{R}\bar{S} + R\bar{S}$	0	1	1	1	0	0	1	0	X	0	X
R Plus S	$\overline{R\bar{S}} + RS$	1	0	0	0	0	0	1	1	0	1	0
S Minus R	$R\bar{S} + \bar{R}S$	1	0	0	1	1	0	0	1	1	1	0
R Minus S	$\bar{R}S + R\bar{S}$	1	0	1	0	0	1	1	0	1	1	0
R Or S	$\bar{R}\bar{S} + \bar{R}\bar{S}$	1	0	1	1	0	0	0	0	X	0	X
R And S	$RS + RS$	1	1	0	0	1	1	1	1	X	1	1
$\bar{R}$ And S	$\bar{R}S + \bar{R}\bar{S}$	1	1	0	1	0	1	0	1	X	1	1
R	$\bar{R}S + \bar{R}\bar{S}$	1	1	1	0	0	1	0	0	X	0	X
R XNOR S	$\bar{R}S + R\bar{S}$	1	1	1	1	0	1	1	0	X	0	X


AD-A119 113
RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV
F/G 9/1
HIGH-SPEED MICRO SIGNAL PROCESSOR.(U)
JUN 82 G AGULE
F33615-77-C-1224
UNCLASSIFIED
BR-13111
AFWAL-TR-82-1071
NL
2 OF 3

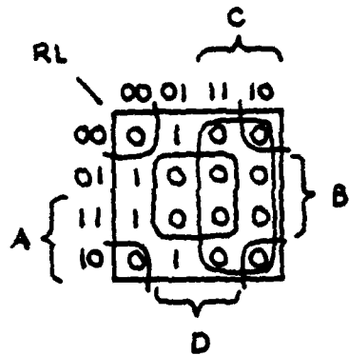
operations to be performed. CS sets all carries, having the effect of making the exclusive -OR gate invert the result from the logic element, changing the equivalent function type from an AND-NOR to an AND-OR. CE takes precedence. The actual mapping of these control signals from the instruction bits is shown in Figure B-1. The resulting equations are summarized in Figure B-2.

The fast-carry inputs to each bit are generated according to the equations in Fig. B-3. Also shown in Fig. B-3 are the equations which define the generate ($\overline{G}$) and propagate ($\overline{P}$) outputs, as well as all other status outputs. A detailed schematic of the MSPALU is found in Figure B-6.

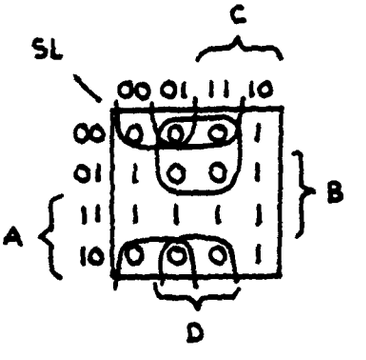
The multiport memory cell is logically similar to the RB-919 (2909M) sequencer memory cell. The difference is that the ALU memory cell has 2 read addresses and a third write address. The transparent latch cell used as the storage element is identical in both memories. The RB-918 memory cell has 2 tri-state buffers on each cell, however. These 2 buffers are enabled by separate address decoding, providing the 2-port output. Also, the write address is separate, being decoded from a third set of addresses. This structure can be seen on sheet 5 of the schematic in Fig. B-6. A penplot of the memory cell and the array capping cells is shown in Figure B-7

1.3 Definition of Signals

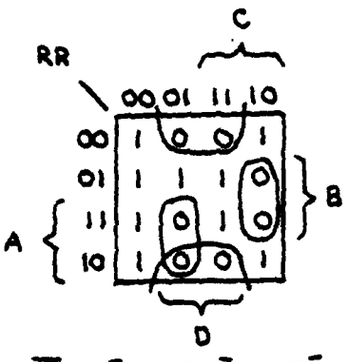
On the following pages is a definition of signals on the RB-918, listed by signal name. An alphabetical cross-reference of signal names and pin numbers follows in Table B-3



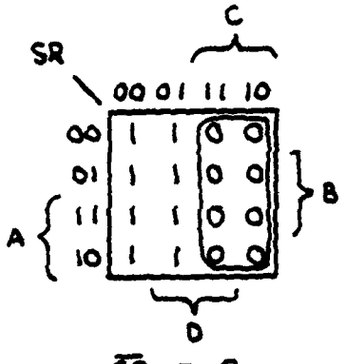
$$\overline{RL} = \overline{C + BD + \bar{B}\bar{D}}$$
$$RL = C + BD + \bar{B}\bar{D}$$



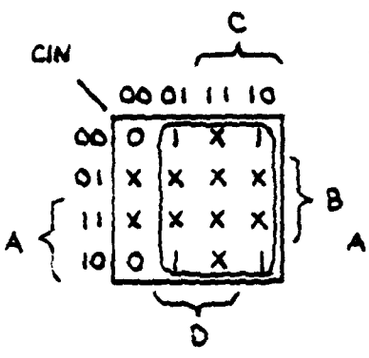
$$\overline{SL} = \overline{\bar{A}D + \bar{B}D + B\bar{C}}$$
$$SL = \bar{A}D + \bar{B}D + B\bar{C}$$



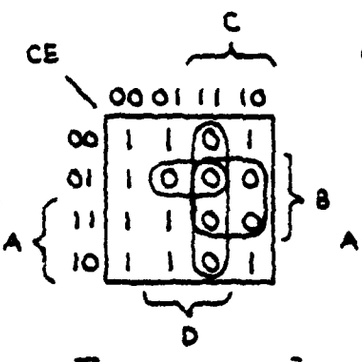
$$\overline{RR} = \overline{\bar{B}D + BC\bar{D} + AD\bar{C}}$$
$$RR = \bar{B}D + BC\bar{D} + AD\bar{C}$$



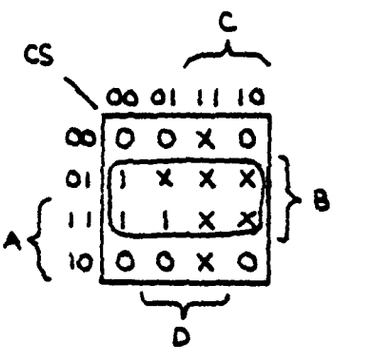
$$\overline{SR} = C$$
$$SR = \bar{C}$$



$$CIN = C + D$$



$$\overline{CE} = BC + CD + \bar{A}BD$$



$$CS = B$$

Figure B-1 ALU Instruction Decode

$$RL = \overline{C + BD + \overline{B}\overline{D}}$$

$$SL = \overline{\overline{A}D + \overline{B}D + B\overline{C}}$$

$$RR = \overline{\overline{B}D + BC\overline{D} + A\overline{C}D}$$

$$SR = \overline{C}$$

$$\overline{CIN} = \overline{C + D}$$

$$\overline{CE} = BC + CD + \overline{A}BD$$

$$\overline{CS} = \overline{B}$$

Figure B-2 Alu Instruction Decode

$G = R\ S$

$P = R + S$

$C_0 = C_0$

$C_1 = C_0P_0 + G_0$

$C_2 = C_0P_0P_1 + G_0P_1 + G_1$

$C_3 = C_0P_0P_1P_2 + G_0P_1P_3 + G_1P_2 + G_2$

$C_4 = C_0P_0P_1P_2P_3 + G_0P_1P_2P_3 + G_1P_2P_3 + G_2P_3 + G_3$

$C_5 = C_0P_0P_1P_2P_3P_4 + G_0P_1P_2P_3P_4 + G_1P_2P_3P_4 + G_2P_3P_4 + G_3P_4 + G_4$

$C_6 = C_0P_0P_1P_2P_3P_4P_5 + G_0P_1P_2P_3P_4P_5 + G_1P_2P_3P_4P_5 + G_2P_3P_4P_5 + G_3P_4P_5 + G_4P_5 + G_5$

$G = G_0P_1P_2P_3P_4P_5P_6P_7 + G_1P_2P_3P_4P_5P_6P_7 + G_2P_3P_4P_5P_6P_7 + G_3P_4P_5P_6P_7 + G_4P_5P_6P_7 + G_5P_6P_7 + G_6P_7 + G_7$

$P = P_7P_6P_5P_4P_3P_2P_1P_0$

$C_8 = C_0P_0P_1P_2P_3P_4P_5P_6P_7 + G_0P_1P_2P_3P_4P_5P_6P_7 + G_1P_2P_3P_4P_5P_6P_7 + G_2P_3P_4P_5P_6P_7 + G_3P_4P_5P_6P_7 + G_4P_5P_6P_7 + G_5P_6P_7 + G_6P_7 + G_7$

<u>ALU OUTPUTS</u>

CARRY OUT = C_8

F EQUALS Ø = FEØ = F0 + F1 + F2 + F3 + F4 + F5 + F6 + F7 + F8

OVERFLOW = OVR = C7 $\oplus$ C8

SIGN BIT = F7

GENERATE = $\overline{G}$

PROPOGATE = $\overline{P}$

DATA OUT = FØ - F7

Figure B-3 Arithmetic Unit Logic Description

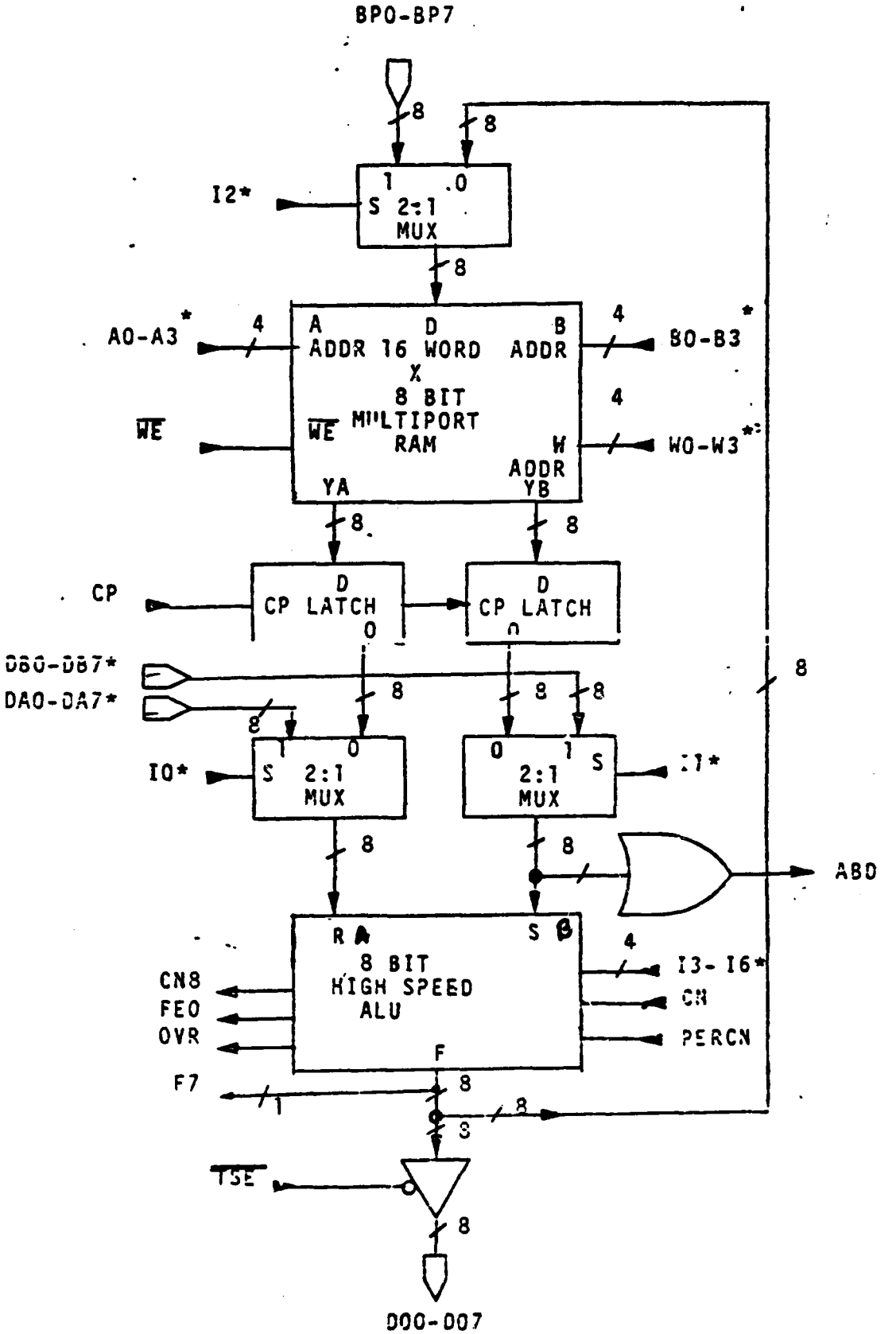


Figure B-4 Device Block Diagram

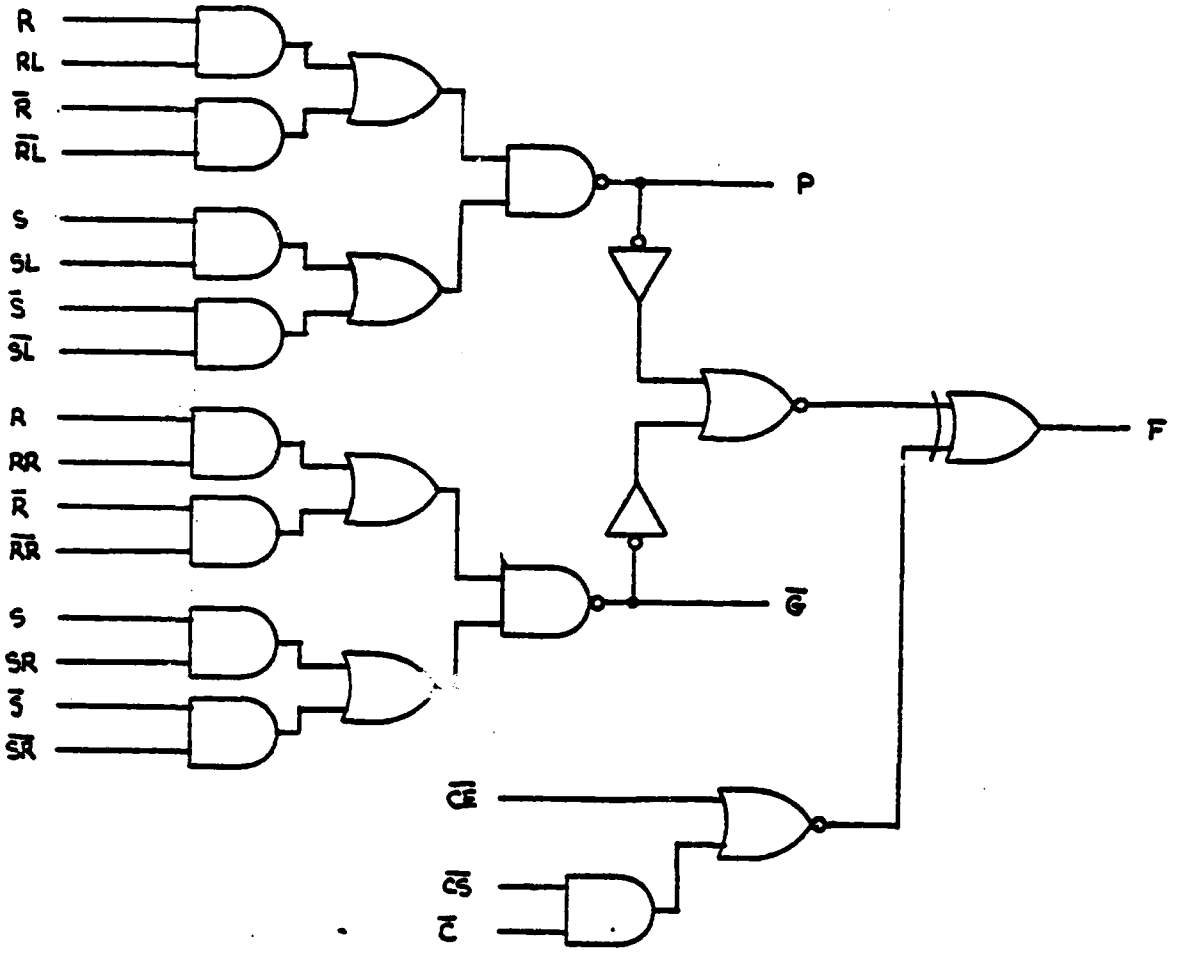


Figure B-5 RB-918 ALU Logic Element

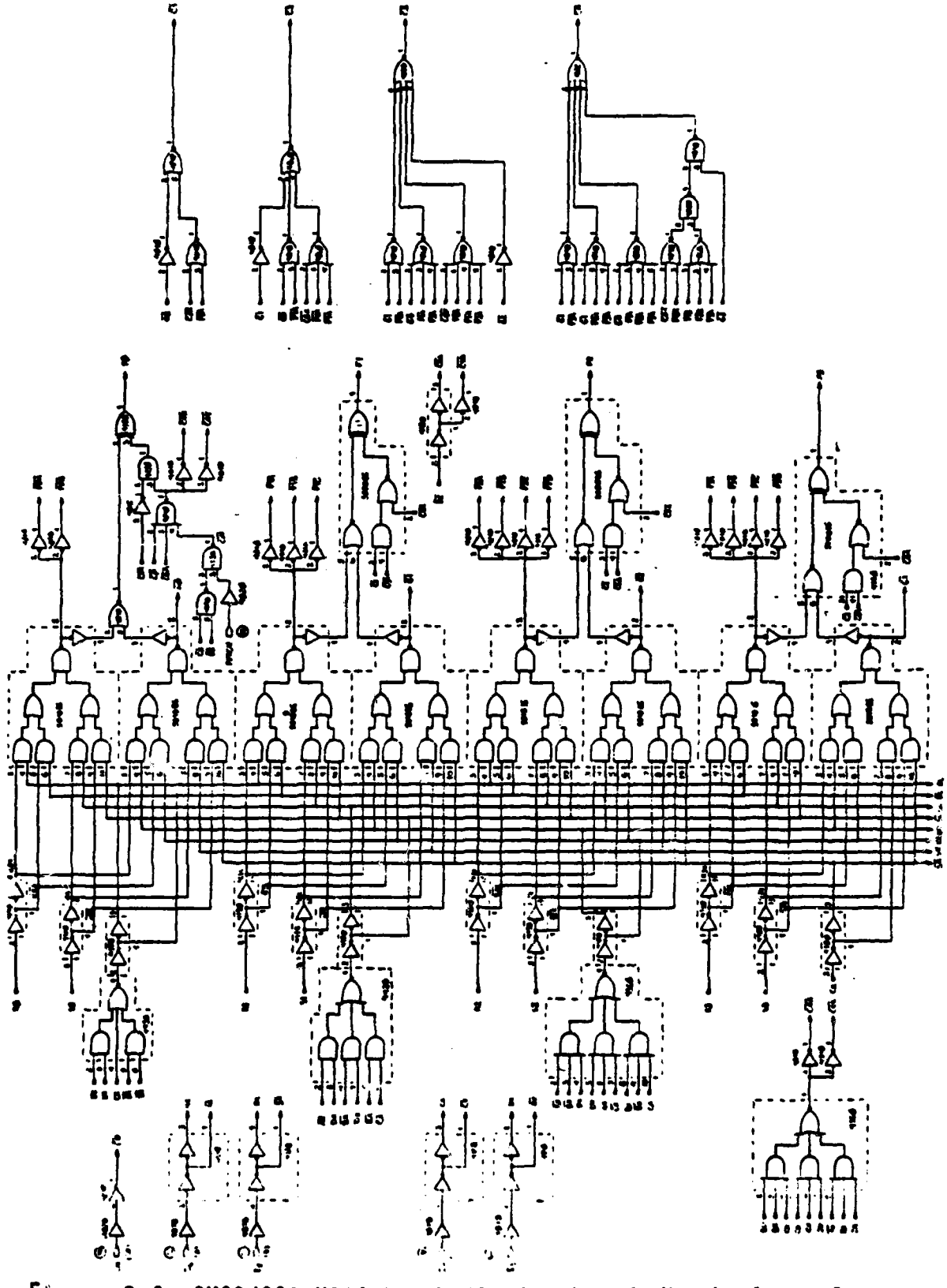


Figure B-6 CMOS/SOS MSPALU RB-918 Arithmetic/Logic Control
(Sheet 1 of 5)

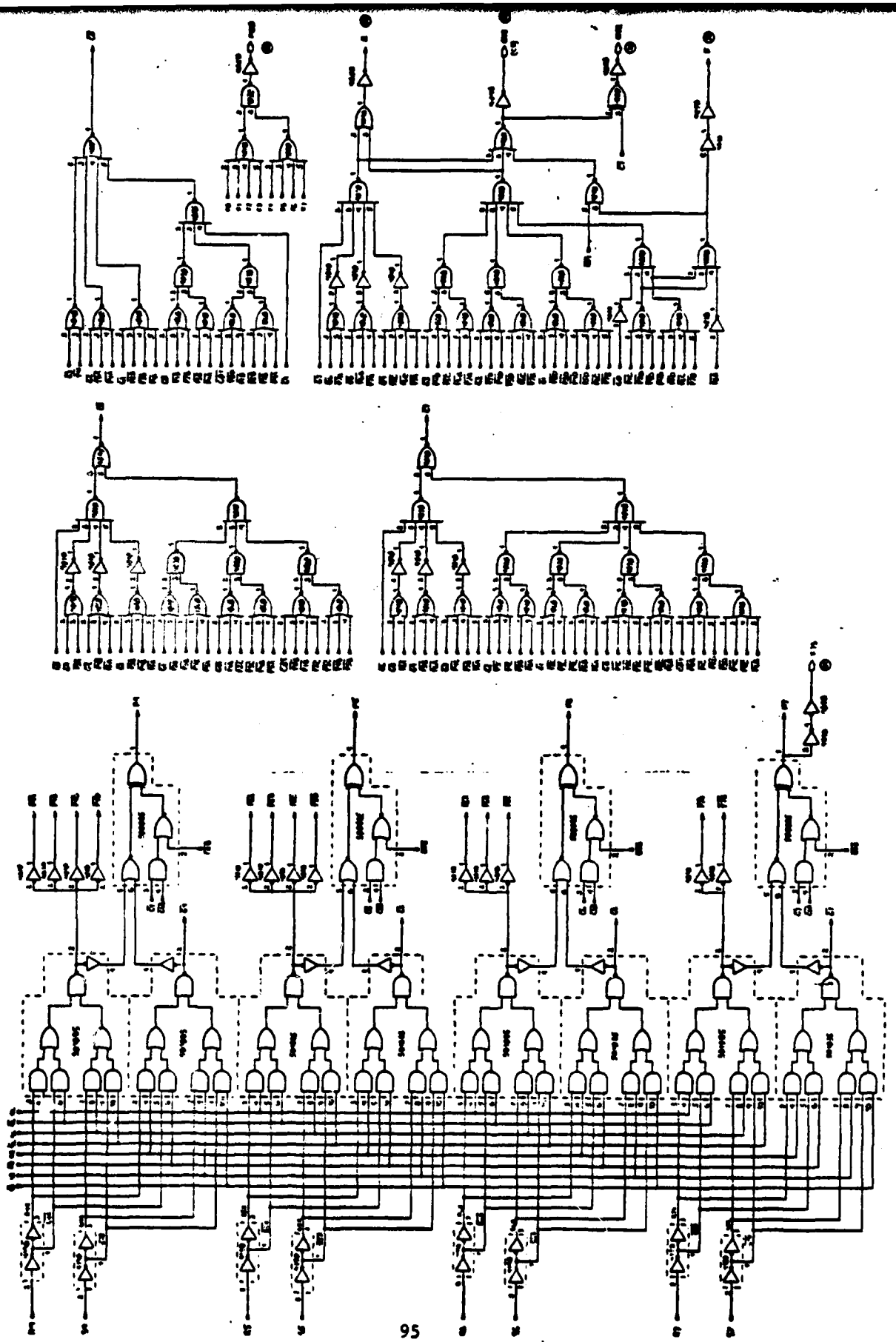


Figure B-6 CMOS/SOS MSPALU R3-918 Arithmetic/Logic Control (Sheet 2 of 5)

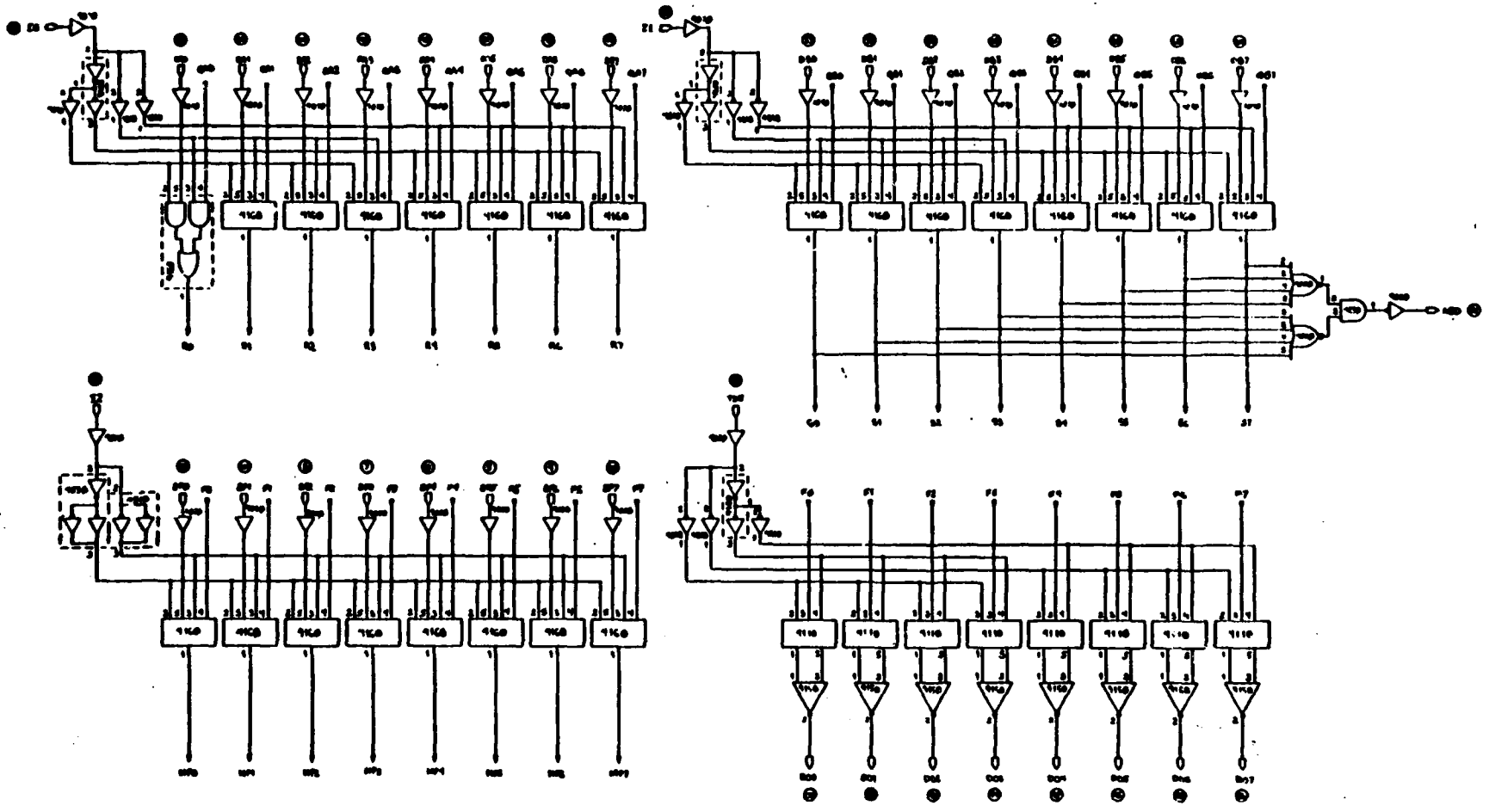


Figure B-6 CMOS/SOS MSPALU RB-918 Data Mulitiplexers and Tri-State Control (Sheet 3 of 5)

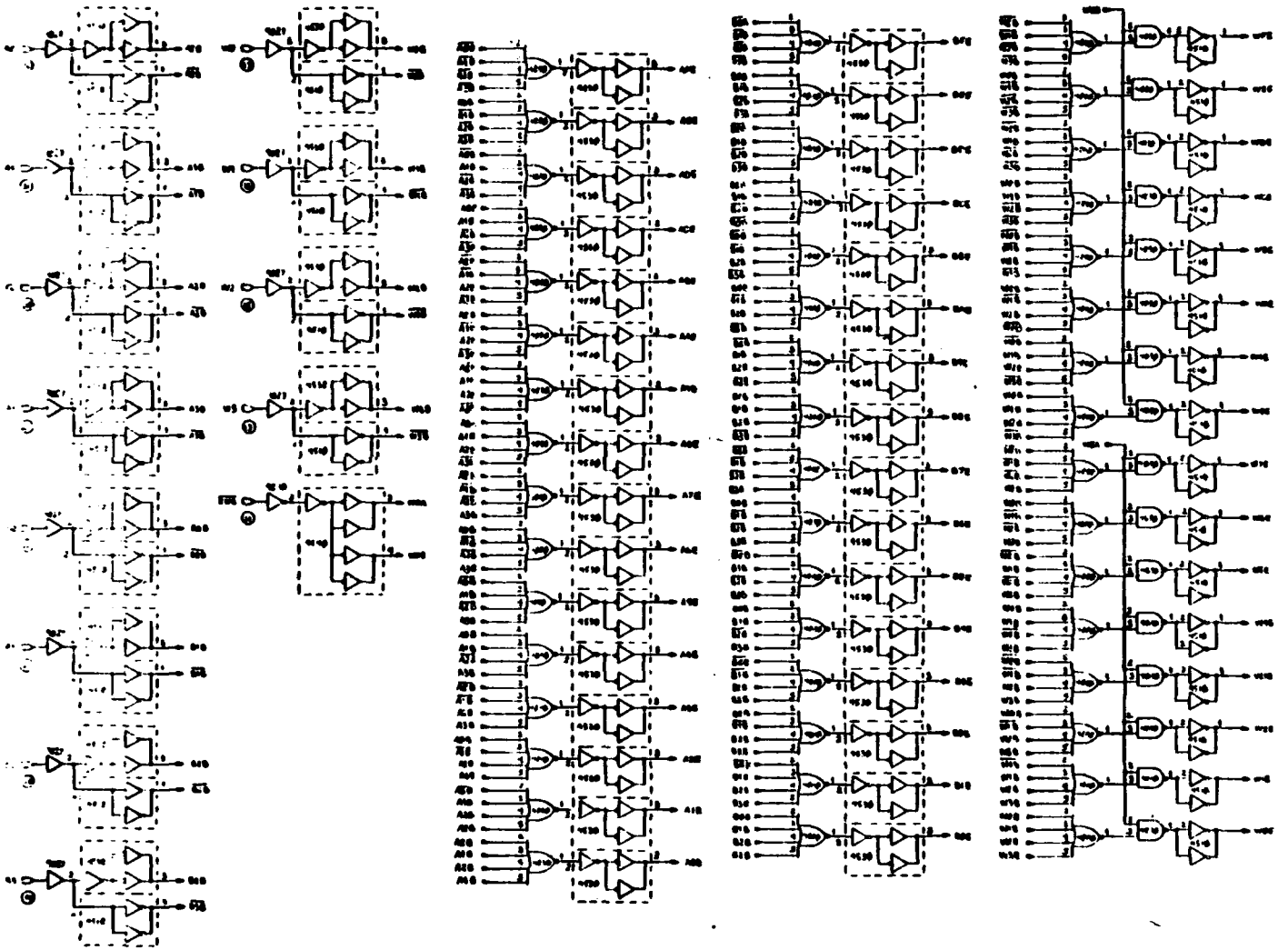


Figure B-6 CMOS/SOS MSPALU RB-918 Multiport Address Decode/Write Control (Sheet 4 of 5)

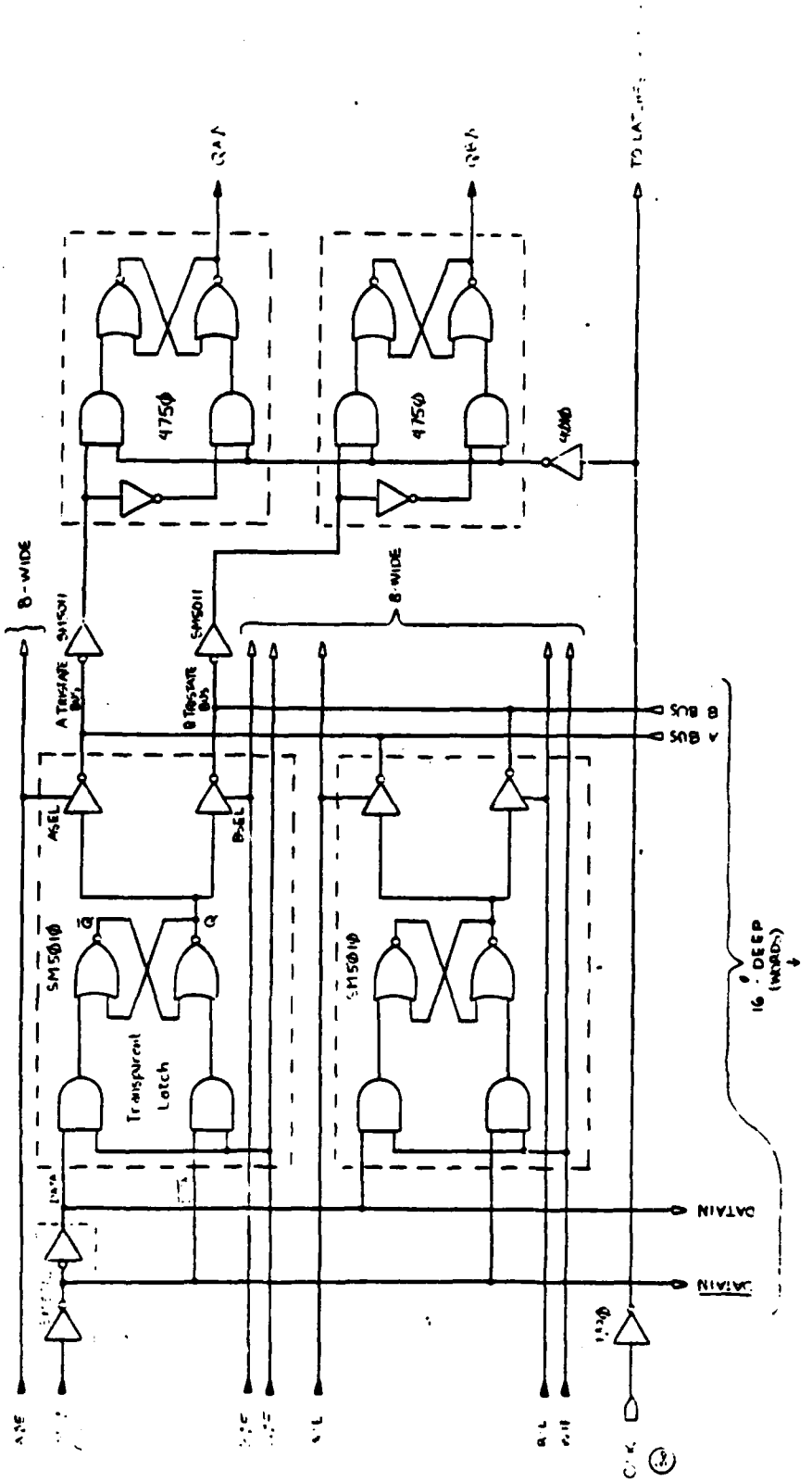


Figure B-6 CMOS/SOS MSPALU ALU Memory Array (Sheet 5 of 5)

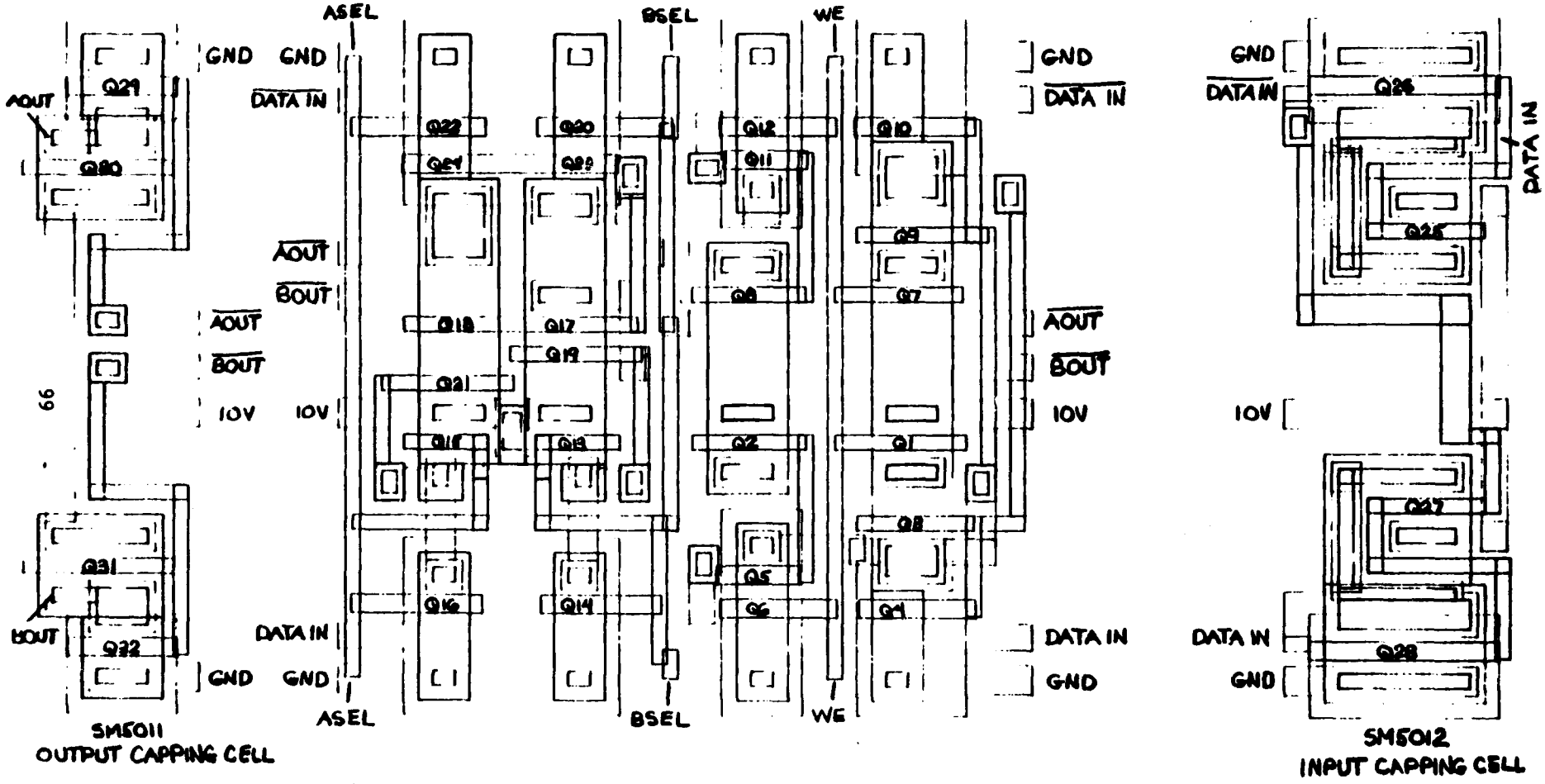


Figure B-7 Multiport ALU Register File RAM Cell SM5010

Those signals marked with an asterisk (*) shall be T^2L compatable when the MSPALU chip is generated at 10V.

Signal Definition

INPUTS

Signal	Function
A0-A3*	4 bit read address for A port of multiport memory.
B0-B3*	4 bit read address for B port of multiport memory.
W0-W3*	4 bit write address for multiport memory.
$\overline{WE}$	Multiport write enable. Logic 0 = write into address specificed by W0-W3.
CLK	Latch enable clock. Logic 0 = hold data, logic 1 = pass data (transparent).
DA0-DA7*	Direct data which may be selected to A port of the ALU. DA0 is the LSB.
DB0-DB7*	Direct data input which may be selected to the B port of the ALU. DB0 is the LSB.
I0*	Control bit for multiplexer ahead of A port of the ALU. Logic 0 selects multiport data. Logic 1 selects external data.
I1*	Control bit for multiplexer ahead of B port of ALU. Logic 0 selects multiport data. Logic 1 selects external data.
I3-I6*	ALU function control as shown in Table B-1.

TABLE B-4
DEVICE RATINGS AND CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	-55°C to +125°C
Non-operating	-65°C to +150°C
Supply Voltage	+15V non-operating
Input Voltage	-.5V to Vcc +.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	-	250	µamp
VOL Output Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input Low	5 10	-	-	1.5 3.0	Volts
VIH Input High	5 10	3.5 7.0	-	-	Volts
IO Outputs Sink and Source	5 10	-	1.5 (within .5V of Supply or GND 1.5		ma
Iin Input Current	0 Ein Vcc	-	.3	1	µamp
Cin data/ clock	any	-	2	3/5	pf
Vcc,	-	4.5	10	12	Volts

Notes: 1. Iin for T^2L ≈200 µA

2. Vin for T^2L - Logic >2.0V
<0.8V

TABLE B-3

SIGNAL-PIN CROSS REFERENCE

SIGNAL NAME	WAFER PIN	PACKAGE PIN	SIGNAL NAME	WAFER PIN	PACKAGE PIN
ABD	51	7	DB5	62	14
A0	32	60	DB6	63	15
A1	31	59	DB7	64	16
A2	30	58	D00	100	36
A3	25	56	D01	98	35
B0	22	55	D02	96	34
B1	21	54	D03	94	32
B2	20	53	D04	92	31
B3	19	52	D05	90	30
BP0	108	37	D96	88	29
BP1	109	38	D07	86	28
BP2	3	41	FE0	83	25
BP3	7	45	F7S	84	26
BP4	6	44	$\overline{G}$	79	--
BP5	5	43	GND	28	57
BP6	4	42	I0	38	62
BP7	102	37	I1	53	9
CLK	36	61	I2	8	46
CN	74	22	I3	69	18
CN8	77	24	I4	70	19
DA0	39	63	I5	71	20
DA1	43	64	I6	72	21
DA2	44	1	$\overline{OVR}$	76	23
DA3	45	2	$\overline{P}$	75	--
DA4	46	3	PERCN	66	17
DA5	47	4	TSE	85	27
DA6	48	5	VCC(+10)	41	33
DA7	49	6	VIN(+5)	106	40
DB0	53	8	$\overline{WE}$	11	47
DB1	58	10	W0	17	51
DB2	59	11	W1	16	50
DB3	60	12	W2	15	49
DB4	61	13	W3	13	48

1.4 Device Characteristics

The static electrical characteristics for the RB-918 are listed in Table B-4. These specifications should be considered as approximate and open for discussion. There are numerous TTL-compatible inputs on the MSPALU. In order for these inputs to actually be TTL-compatable however, it is necessary to connect Vin to a 5-volt supply. Connecting Vin to a 10-volt supply will cause these inputs to be 10V compatable however with considerably different characteristics than regular 10V only CMOS/SOS inputs. Most notably, the threshold for switching will remain at the TTL level of about 1.6 volts. This is due to the characteristics of the RB9070 programmable 5/10V input cell. Also, the input will source current when low, as is characteristic of a TTL input. Specifically, it should source on the order of 200 µamp when low.

Since the RB-918 is primarly a combinational circuit, the switching characteristics are determined by worst-case propogation delays. In this instance, the worst-case is an operation where 2 operands are read from memory, an operation is performed and resultant data is written back to memory during 1 cycle. This must be accomplished in 150 nsec or less.

1.5 Bonding

The bonding diagram for the RB-918 MSPALU is given in Figure B-8. This bonding diagram is now considered fairly firm for the purpose of system configuration.

OUTPUTS

Signal	Function
A8D	Logical 'OR' of the 8-bits ahead of the 8 port of the ALU.
CN8	Ripple-carry out of ALU.
FEO	Logical 'NOR' of ALU output detects all zeros.
OVR	Overflow. This is the 'Exclusive - 'OR'' of the ALU MSB's carry in and carry out. This bit = logic 1 indicates 2's complement operation has overflowed.
F7	This is the most significant bit out of the ALU.
DØØ-DØ7	Data output of chip. DØØ is the LSB.
VCC	Power
VIN	5 volts for TTL input.
GND	Return

TOTAL PIN USAGE = 64

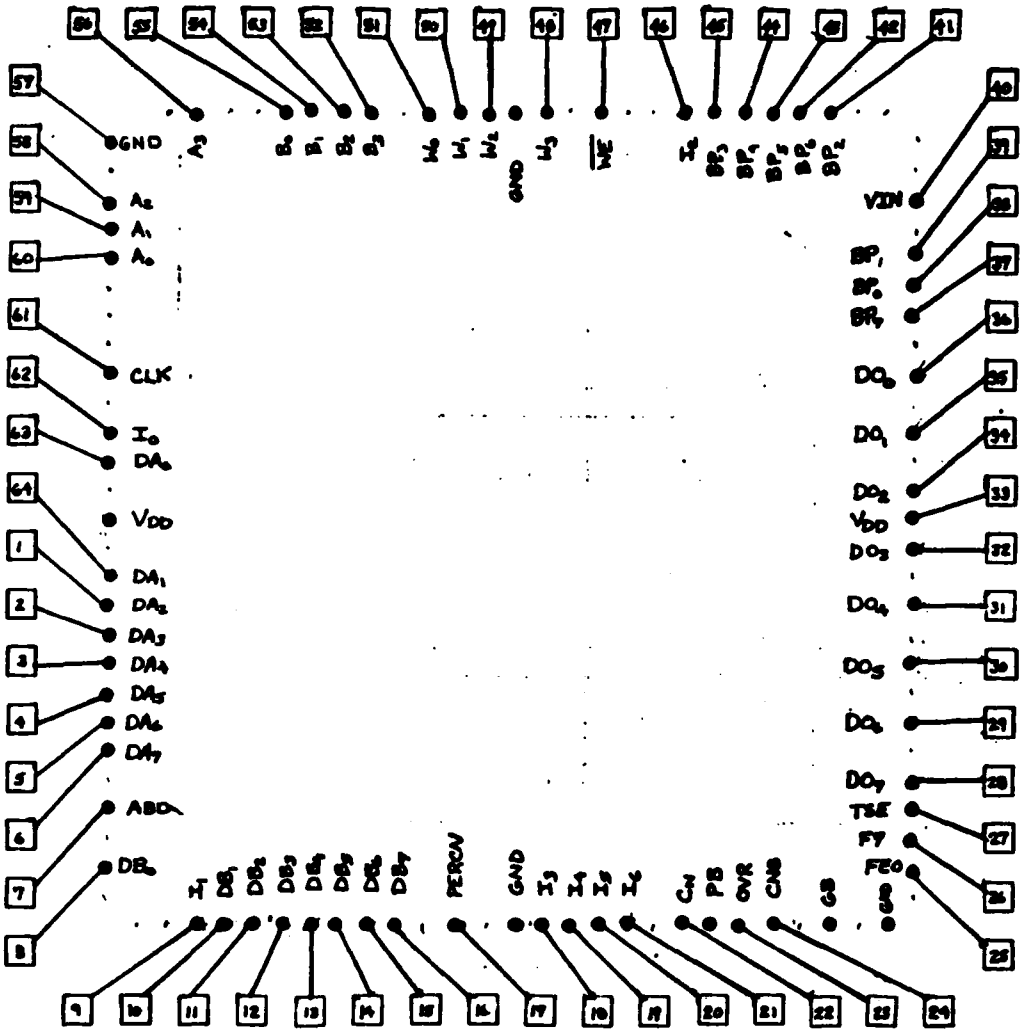


Figure B-8 MSPALU (RB918) Bonding

APPENDIX C

2909M DEVICE DESCRIPTION AND SPECIFICATION

1.0 GENERAL DESCRIPTION

The 2909M or RB-919 microprogram sequencer is a functional equivalent of the AM2909, except that the stack on the 2909M is 16 words deep. The stack on the AM2909 is only four words deep. A block diagram of the 2909M is shown in Fig. C-1. As in the AM2909, the 2909M can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs which is stored in an internal register; 3) a 16-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one).

Stack operations are controlled by the PUSH/POP and FILE ENABLE inputs. The address selection is controlled by the select inputs S_0 and S_1. Fig. C-6 shows the truth table for these four lines. The OR inputs are used to force address bits into the Y outputs. Each OR_i input bit is logically ORed with the corresponding bit in the input selected by the address multiplexer. Also, a $\overline{ZERO}$ input is provided to force all Y outputs to zero when low. The output control $\overline{OE}$ is a tristate enable. When $\overline{OE}$ is high, the outputs are in the high-impedance state (disabled).

The 4-bit 2909M may be cascaded to achieve wider addresses. Successive stages are cascaded by connecting the carry-out of the less-signficant stage to the carry-in of the next-most-significant stage. Lookahead carry is provided within each state, and ripple carry is used between stages.

1.1 Operation of the 2909M

Because there are four inputs to the multiplexer, there are basically four major types of operations that can be performed. The first two are very straightforward and require little explanation. These are: 1) use of direct inputs and 2) use of internal holding register. In the first case data appearing directly on the D-inputs will be passed to the Y outputs. In the second case data brought in through the R-inputs and stored in the register can be passed to the output. This register is loaded on the clock LOW to HIGH transition if the register enable signal $\overline{RE}$ is low.

A third multiplexer input is the PC or program counter register. The input to the PC register is an incrementer. The incrementer essentially adds the carry-in (Cn) input to the current Y output. Therefore, if the least significant Cn is high, the PC register will be loaded with the current Y output word plus 1 (Y+1→μPC). If Cn is low, the Y output will be loaded into the PC register unchanged on the next clock LOW to HIGH transition.

The last source available at the multiplexer input is a 16x4 stack. This stack is used to provide return address linkage when executing micro subroutines or servicing interrupts. A built-in stack pointer always points to the last file word written. This allows the address on the top of the stack to be referenced without a PUSH or POP. The stack pointer is essentially an up/down counter controlled by the push/pop (PUP) and file enable ($\overline{FE}$) inputs. When $\overline{FE}$ is low and push/pop is high, a PUSH operation will occur. This means that the stack pointer will first be incremented to the next stack address and then the current contents of the PC register will be written there. At this time the PC register should contain the next microinstruction address following the subroutine jump which initiated the PUSH.

If $\overline{FE}$ is low and the push/pop control is low, a POP operation occurs This implies the usage of the return linkage during this cycle and consequently a return from subroutine or return from interrupt. The stack pointer will be decremented on the next LOW-to-HIGH clock transition. If the file enable ($\overline{FE}$) is HIGH, the stack pointer remains unchanged regardless of any other input.

The $\overline{ZERO}$ input is used to force the four Y outputs to zero when low, regardless of any other input. Each Y output also has a separate OR input which allows a logic one to be forced at each cutput. The output enable ($\overline{OE}$) is a tristate control. When $\overline{OE}$ is high, the Y outputs are in the high impedance state. Figures C-6 thru C-10 are taken from the AM2909 data sheet by Advanced Micro Devices. The tables on these pages illustrate the operation of the 2909M under various states of input conditions.

1.2 Logic Implementation

Several areas of the 2909M logic warrant further explanation, in particular, the stack control logic and the incrementer. The incrementer is basically a lookahead carry adder which is simplified since one operand is always either one or zero. The carry-in (Cn) is added to the Y output. Therefore, setting the least-significant carry-in will cause the Y output to be incremented by one and stored in the PC register. If the carry-in is not set, zero is added and the Y output passes to the PC register unchanged.

The stack control logic is designed to keep all operations completely synchronous with the clock. Since a PUSH operation requires incrementing the pointer before writing, and the POP operation requires decrementing after reading, there is a lack of symmetry in these two operations. This can be overcome quite easily, however, if both the inputs and the outputs of the stack pointer flip-flops are utilized (see Schematic, Fig. C-2). Since the inputs and outputs of these flip-flops are separated by one clock cycle, the input will always be either one more or one less than the output during a PUSH or POP operation. By multiplexing these two signals to form the actual stack pointer a useful function can be achieved. When doing a PUSH operation, the UP/DOWN counter is set to count up. This means that the input to the flip-flops is equal to the output plus one. This effectively increments the pointer at the beginning of the cycle. Also, if the input is used as the stack pointer, the location pointed to by the output after the next clock cycle will be written. If the output is selected during a POP operation, the stack pointer will contain the address of the location just written, and will get decremented after the POP operation, on the next LOW tc HIGH transition of the clock. This allows the stack pointer to always point to the current top-of-stack. In this way the stack pointer always gets changed at the end of a PUSH or POP cycle by the next LOW to HIGH clock transition. However, the effective stack pointer at the output of the RB-4170 muxes, gets incremented before writing and decremented after reading as desired. (See also Figure C-13).

Another area of the stack control logic of note is the stack memory data input. It was found during simulation that a critical timing path was present in the write control to the stack memory. As can be seen in the timing diagram (Fig. C-3), it is important that the write signal goes away before a new PC value appears at the stack memory input. Otherwise, the new value of PC will be written into memory, instead of the value that it is wished to PUSH. The logic was implemented such that the memory is written during every cycle. However, only during a PUSH operation is a new value stored. At all other times the location addressed is written with the data already contained, there, so the net effect is no change. This allows the minimum possible delay between the system clock and the write signal helping to assure that the write signal will disappear before the clock LOW-to-HIGH transition can change the data in the PC register. For testing purposes, the relationship between the memory write signal and the PC register data is still considered to be critical, although the likelihood of a problem occurring here is significantly reduced with the current scheme. The necessary timing relationship is indicated in Figure C-3.

A detailed plot of one stack memory cell is shown in Fig. C-4. Input and output capping cells are also shown. In constructing the memory array, this cell is repeated 64 times. It is mirrored both horizontally and vertically. Figure C-5 illustrates a shortened row of memory cells with the caps on either side. This row contains only four cells, rather than 16, but shows how the cells are mirrored to overlap VCC and GND. It also shows the capping cells in place. In addition to the horizontal mirroring of cells, the rows are mirrored in the vertical direction. A common ground can be used between pairs of rows. A total of four rows is used, each being a mirror of the adjacent row. The ENABLE ($\overline{EN}$) and WRITE (W) lines from the select logic in Fig. C-2 connect to the memory as illustrated in Figure C-5. The data inputs and outputs appear at the ends of the memory and are buffered via the capping cells.

1.3 Definition of Signals

INPUTS:

S_0, S_1	Control lines for address source selection as defined in Figure C-6

INPUTS:

$\overline{FE}$	File enable - allows manipulation of stack for PUSH or POP operations when low.
PUP	PUSH/POP control - when PUP is high, a PUSH operation will occur, when low a POP occurs.
$\overline{RE}$	Register enable - enables loading of internal register when low.
OR_{0-3}	Logic OR inputs on each address output line.
$\overline{ZERO}$	Forces all Y outputs to zero when low.
$\overline{OE}$.	Output tristate enable - active low.
C_n	Carry-in to the incrementer.
R_{0-3}	Inputs to the internal address register.
D_{0-3}	Direct inputs to the multiplexer.
CP	Clock input to all clocked interal registers.

OUTPUTS:

Y_i	Address outputs from 2909M.
Cn+4	Carry out from the incrementer.

INTERNAL SIGNALS:

SPØ-SP3	Stack pointer for PUSH/POP stack.
$\overline{PCØ}$-$\overline{PC3}$	Inputs to stack memory (equal to inverted PC register contents during PUSH operation).
RFØ-RF3	Outputs from stack memory.
WØ-W15	Write signals to each stack memory location.
$\overline{ENØ}$-$\overline{EN15}$	Read enable signals to each stack memory location.

1.4 Device Characteristics

The static electrical characteristics for the 2909M are listed in Fig. C-11. These specifications should be considered as approximate, and open for disccusion.

The switching characteristics of the 2909M should meet the specifications for the AM2909 as given in the Advanced Micro Devices data sheet in Fig. C-10. It is desired that the devices meet the commercial specifications over the military temperature range.

1.5 Bonding

The tentative bonding diagram for the 2909M is given in Fig. C-12. Again, this is open for modification if necessary.

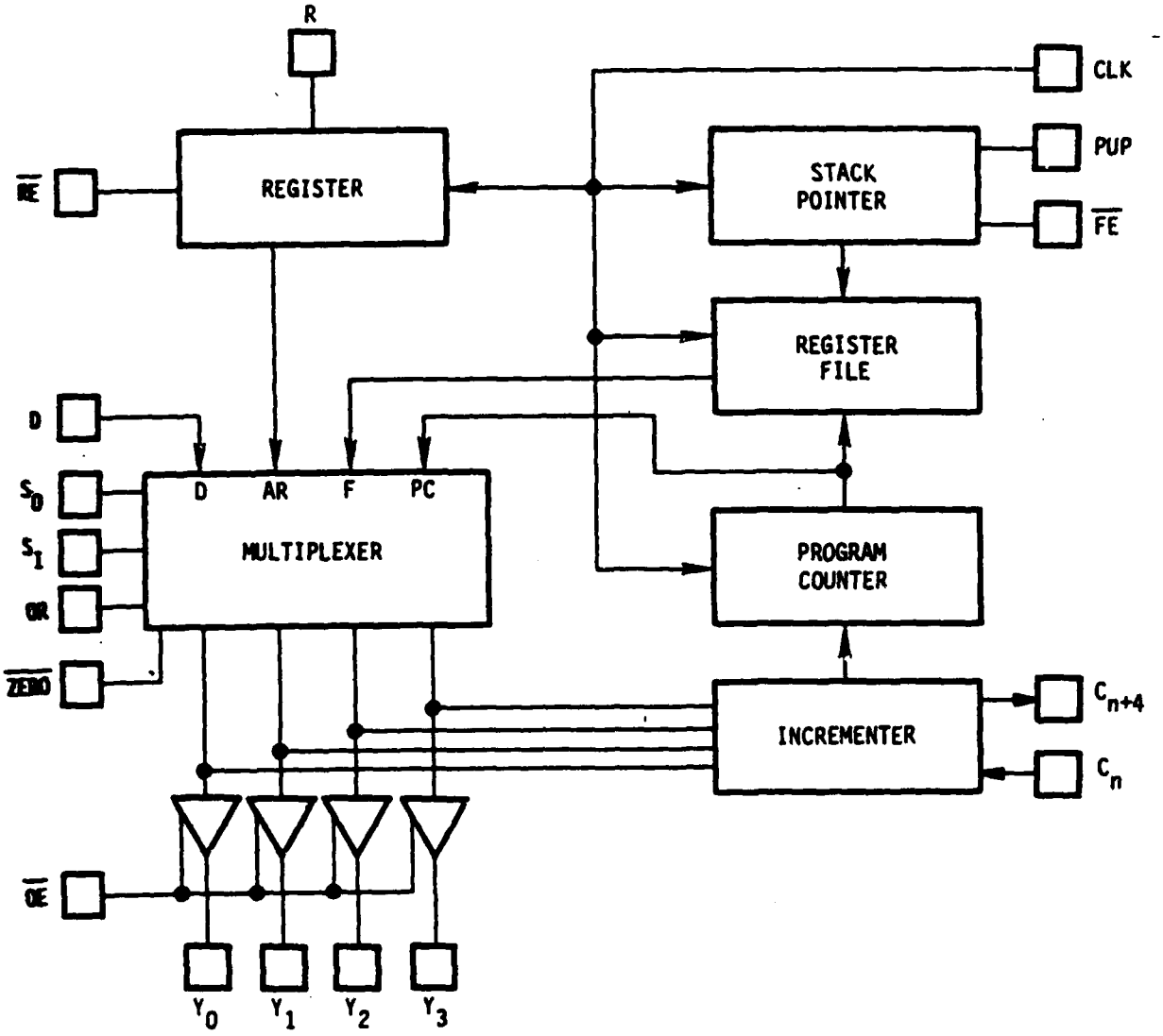


Figure C-1 2909 (RB-919) Block Diagram

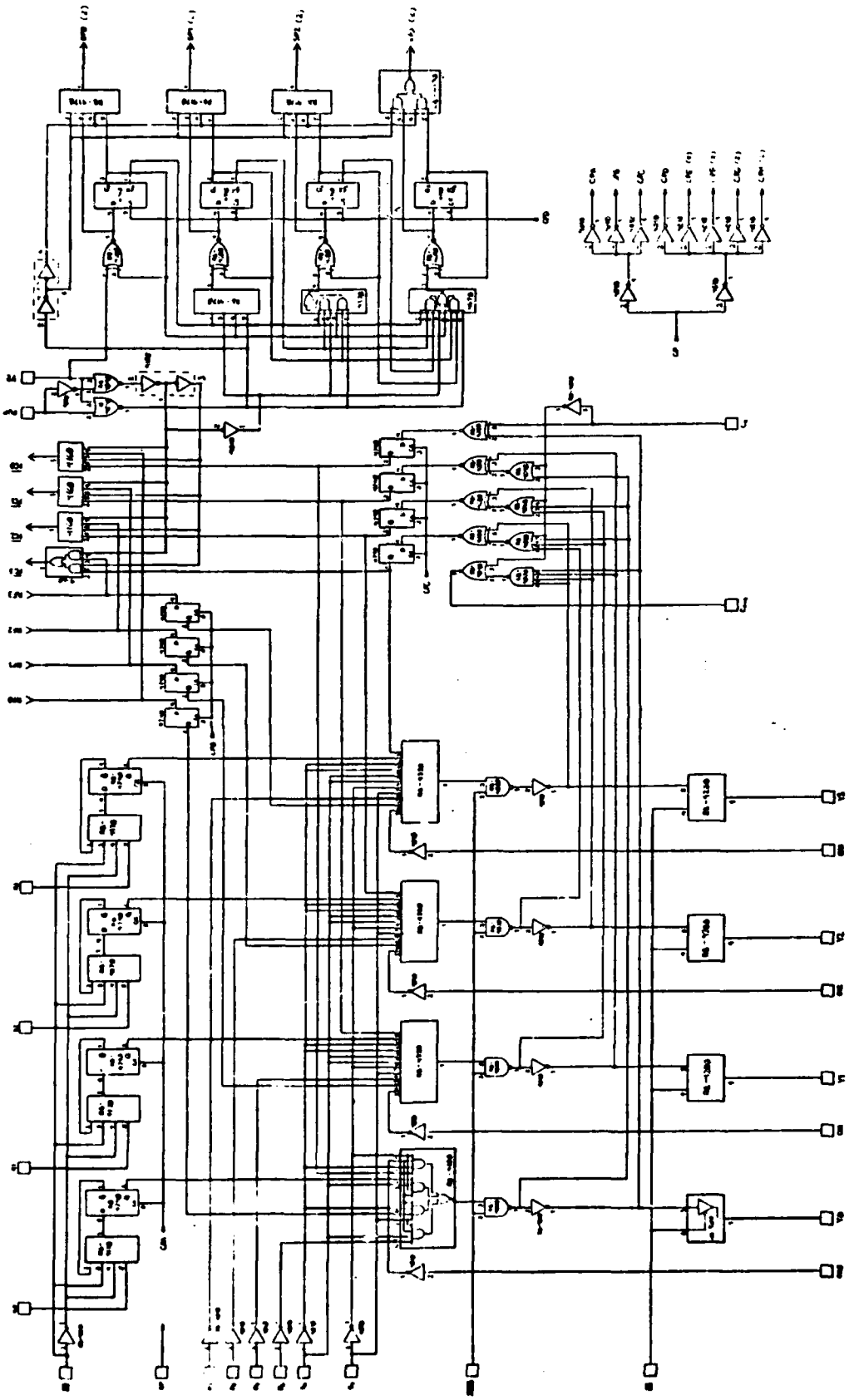


Figure C-2 CMOS/SOS Micro Program Sequencer 2909M (RB-919) (Sheet 1 of 2)

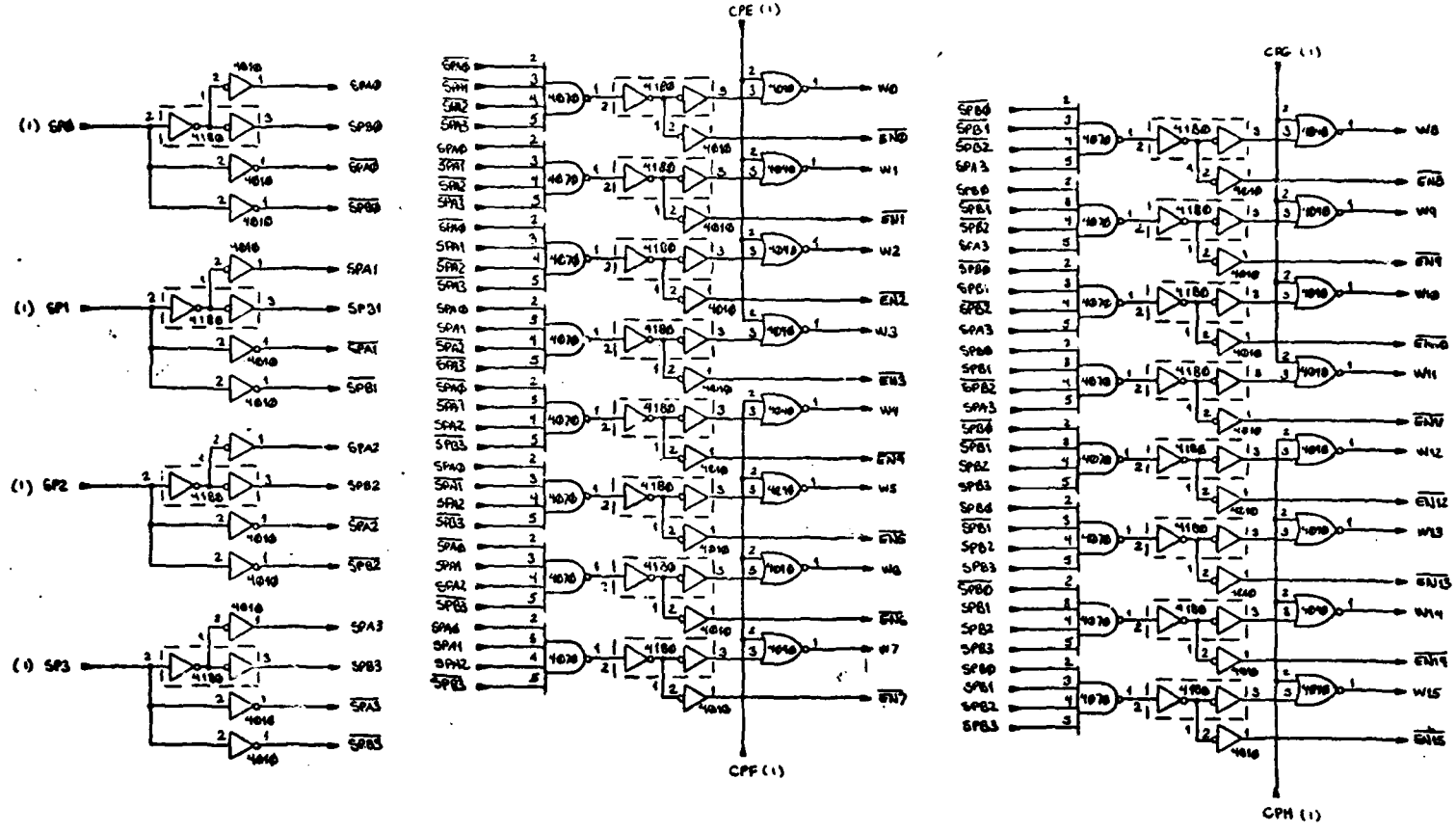


Figure C-2 CMOS/SOS MICROPROGRAM SEQUENCER 2909M (RB-919) MEMORY ADDRESS DECODE

(Sheet 2 of 2)

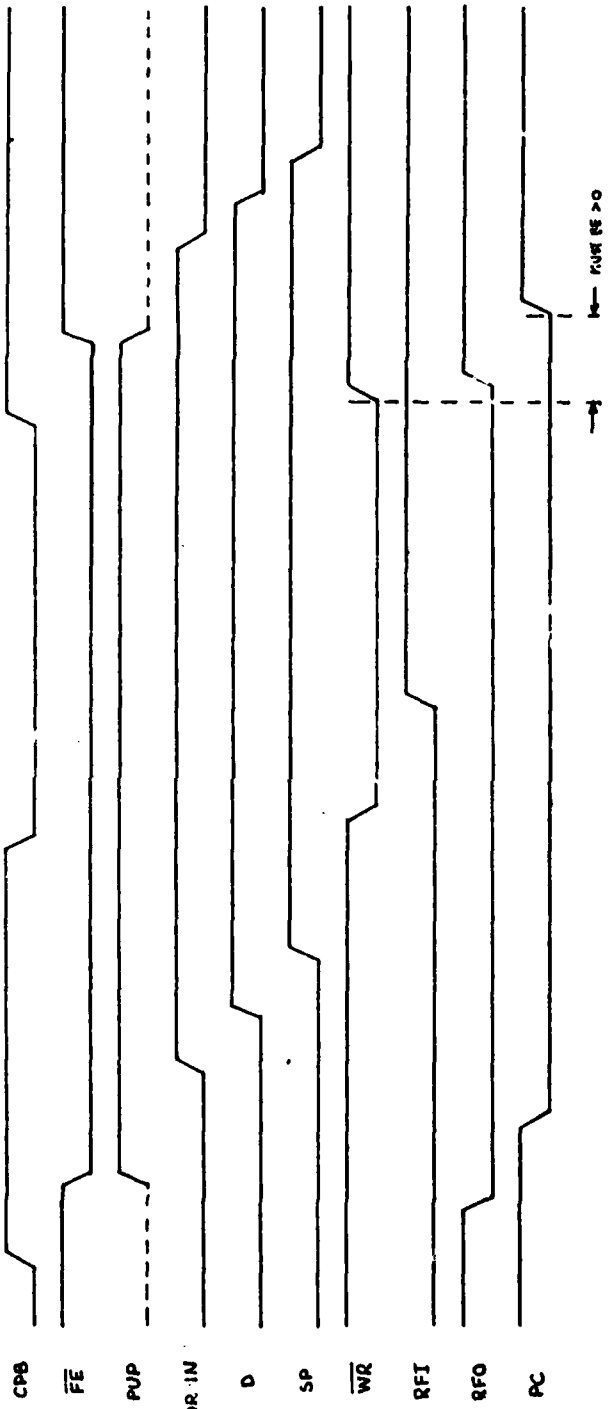


Figure C-3 2909M Push Timing

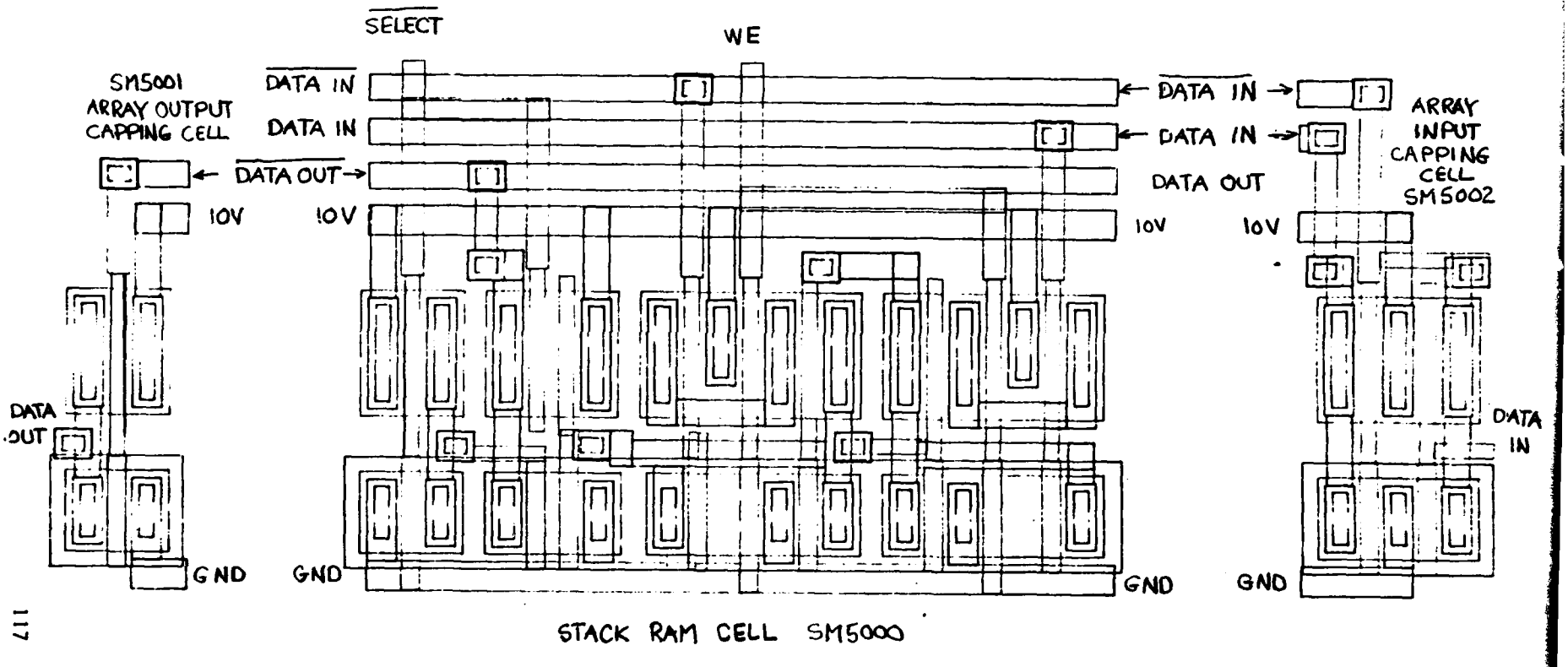


Figure C-4 Stack RAM Cell

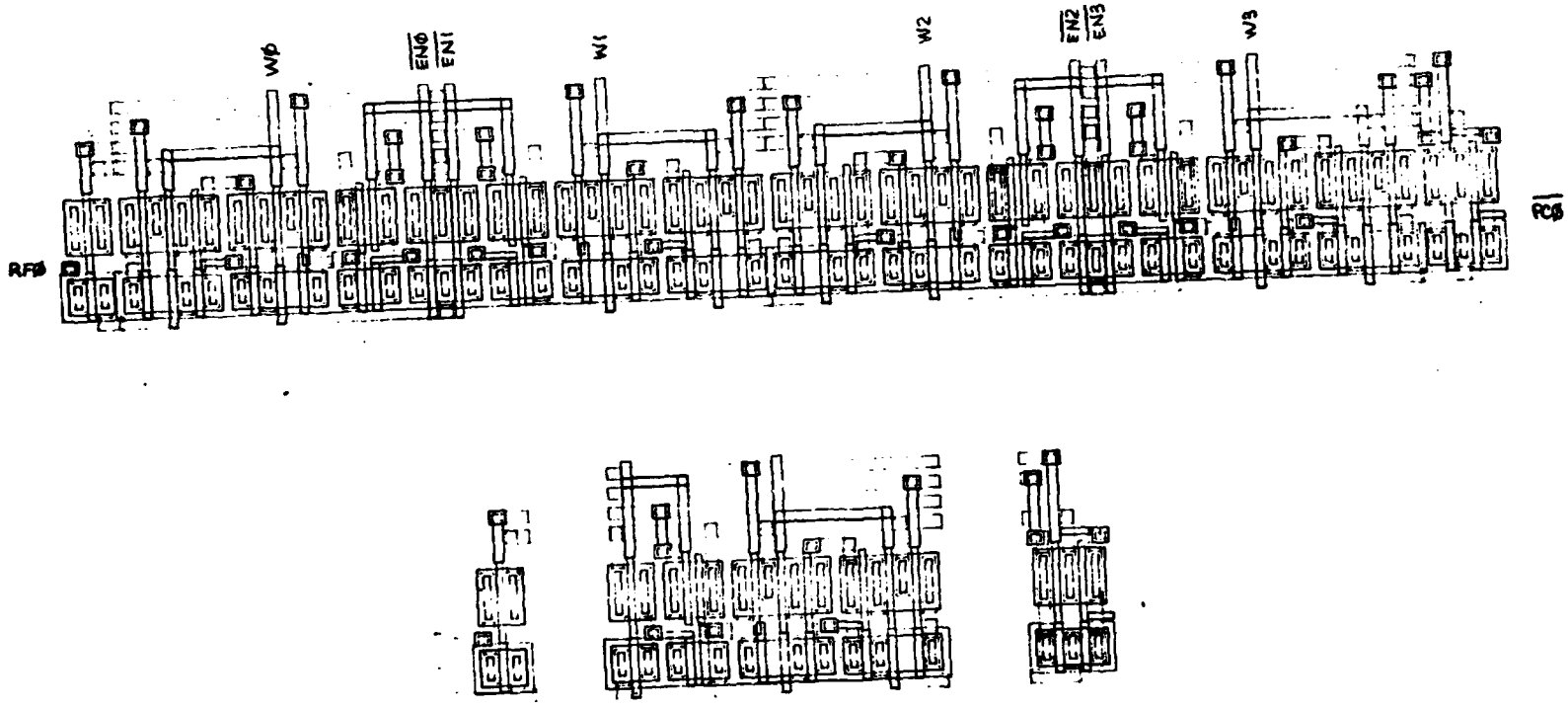


Figure C-5 Memory Cells

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

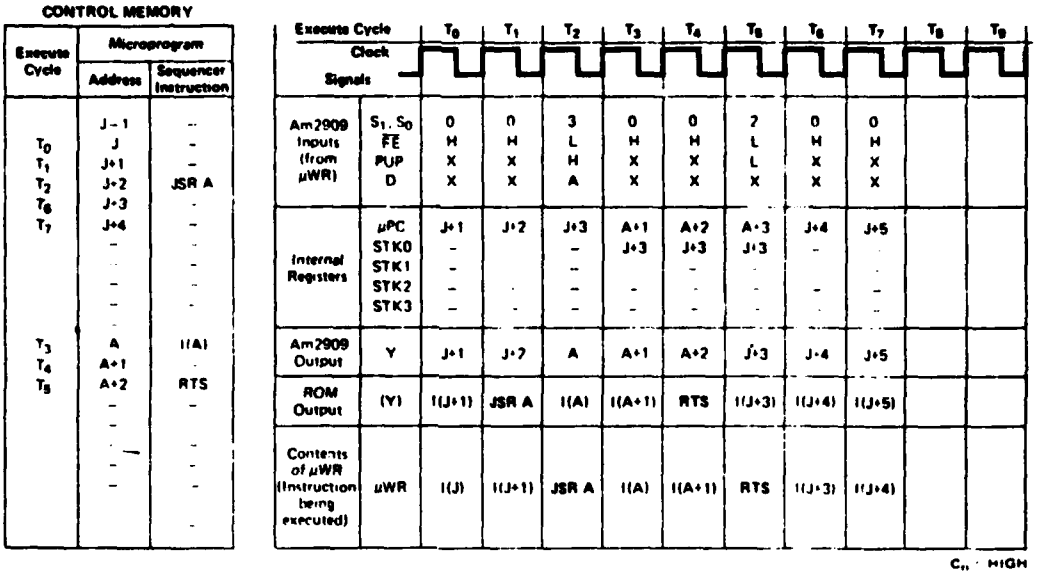
H = High
L = Low
X = Don't Care

Figure C-6 Synchronous Stack Control

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D	Jump to Address on D	JMP D

X = Don't care. 0 = LOW, 1 = HIGH. Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer

Figure C-7 Output and Internal Next-Cycle Register States for Am2909/Am2911



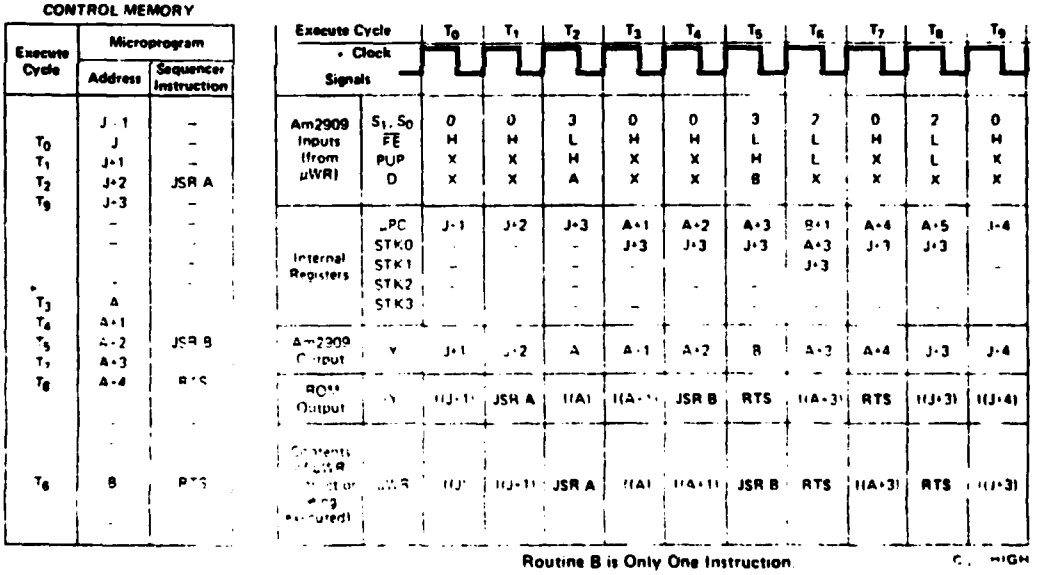
CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_3	J+3	–
T_4	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_5	A	I(A)
T_6	A+1	–
T_7	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle / Clock / Signals		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Am2909 Inputs (from µWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	µPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–		–	J+3	J+3	J+3	–			
	STK1	–		–		–					
	STK2	–		–	–	–	–	–	–		
	STK3	–		–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of µWR (Instruction being executed)	µWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

C_n = HIGH

Figure C-8 Subroutine Execution



CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_3	J+3	–
T_4	A	–
	–	–
	–	–
	–	–
T_5	A+1	–
T_6	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
T_9	B	RTS
	–	–

Execute Cycle / Clock / Signals		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Am2909 Inputs (from µWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	µPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–		–	–			J+3			
	STK2	–		–	–	–	–	–	–	–	
	STK3	–		–	–		–	–	–	–	
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of µWR (Instruction being executed)	µWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

Routine B is Only One Instruction

C_n = HIGH

Figure C-9 Two Nested Subroutines.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the Am2909 and Am2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 5[illegible]pF, except output disable tests)

From Input	COMMERCIAL Y	COMMERCIAL C_{n+4}	MILITARY Y	MILITARY C_{n+4}
D	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n		14		16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25		25	
$\overline{OE}$ HIGH (disable)	25		25	
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

Operating Range	*Part Numbers*	*Power Supply*	*Temperature Range*
Commercial	Am2909PC, DC Am2911PC, DC	5.0V ± 5%	T_A = 0°C to +70°C
Military	Am2909DM, FM Am2911DM	5.0V ± 10%	T_C = −55°C to +125°C

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL Set-Up Time	COMMERCIAL Hold Time	MILITARY Set-Up Time	MILITARY Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		26	5	30	5
D_i	2	30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.

Figure C-10 Switching Characteristics Over Operating Range

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	-55°C to +125°C
Non-operating	-65°C to +150°C
Supply Voltage	+15V non-operating
Input Voltage	-.5V to Vcc +.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	-	250	µamp
VOL Output Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input Low	5 10	-	-	1.5 3.0	Volts
VIH Input High	5 10	3.5 7.0	-	-	Volts
IO Outputs Sink and Source	5 10	-	1.5 (within .5V of Supply or GND 1.5		ma
Iin Input Current	0 Ein Vcc	-	.3	1	µamp
Cin data/ clock	any	-	2	3/5	pf
Vcc,	-	4.5	10	12	Volts

Notes: 1. Iin for T^2L ≈200 µA

2. Vin for T^2L - Logic $\geq$2.0V
$\leq$0.8V

Figure C-11 Absolute Maximum Ratings

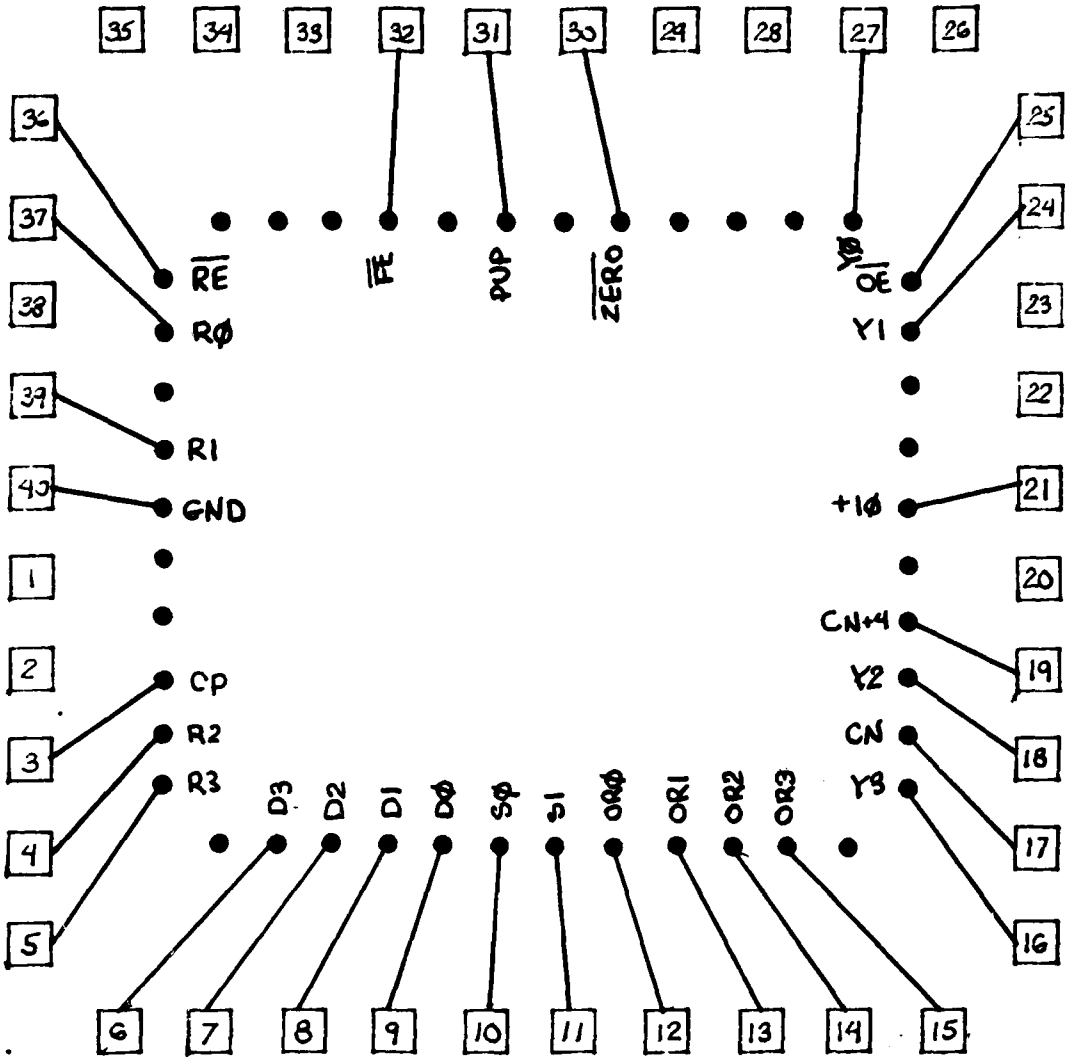


Figure C-12 2909M (RB-919) Bonding

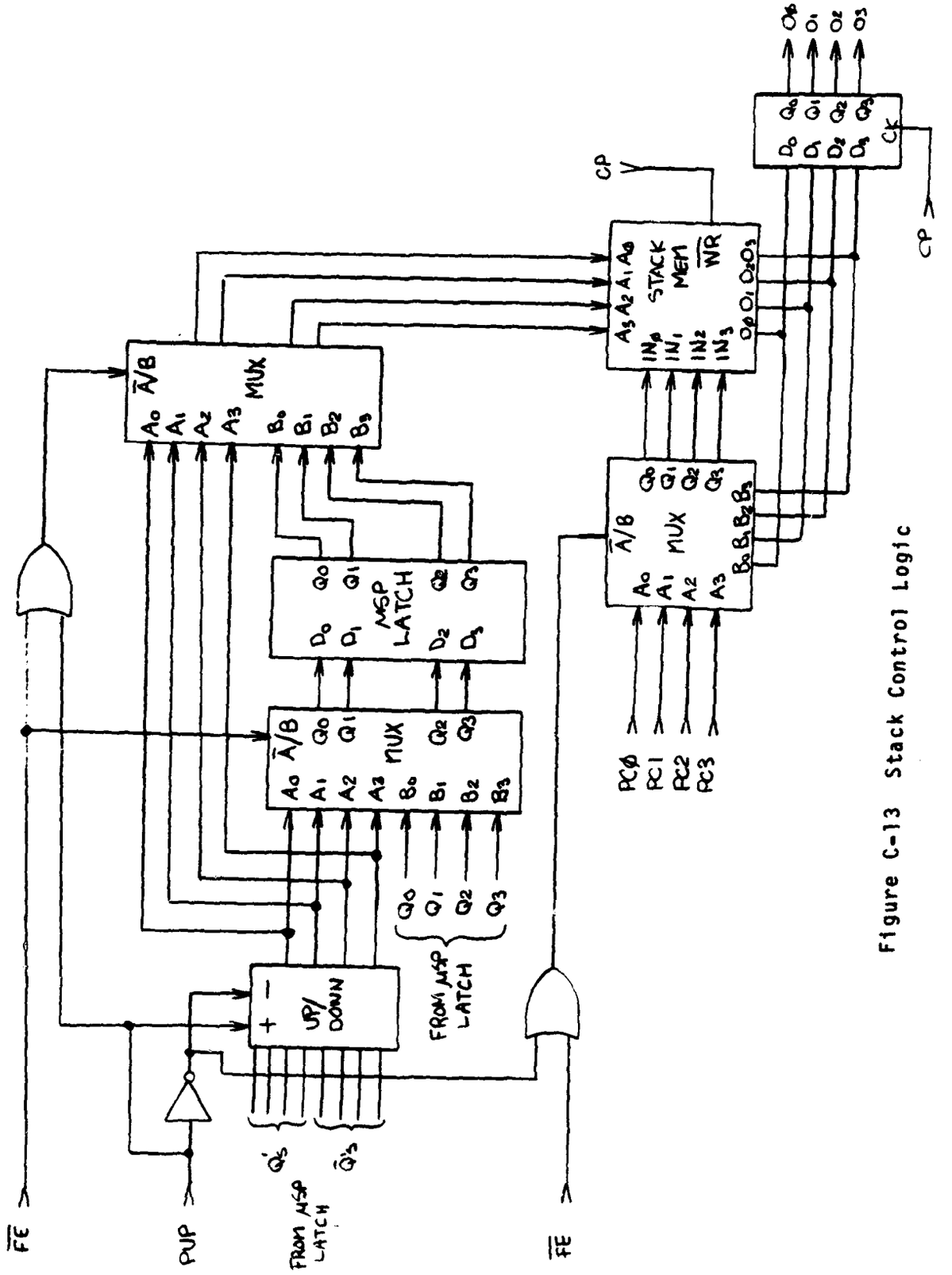


Figure C-13 Stack Control Logic

APPENDIX D

TCS140 DESCRIPTION

1.0 DETAILED DESCRIPTION OF TCS140

1.1 Functional Description

The TCS140 is a two clock delay 12 bit by 12 bit binary multiplier that produces a 24 bit product in less than 150 ns. The multiplier design allows signed and unsigned arguments to be handled depending on control inputs in a basic 2's complement arithmetic number scheme for single and double precision operations.

A block diagram of the multiplier is shown in Fig. D-1. For discussion, the array consists of five separate logic groups, namely, two retiming registers, a decoding and partial adder, a final adder, and output tristate drivers.

The input arguments to the multiplier are the Multiplier, MULTB, and the multiplicand MULTA. These inputs are temporarily stored on the multiplier array by action of the first level of retiming. The outputs of the retimers feed the decoding section where the basic operations required by the multiplication algorithms are performed. In the decoding section the 12 bits of the multiplier, MULTB, are decoded two bits at a time from the least significant, MULTB(11) to the most significant MULTB(0). The decoding of the two adjacent bits determine whether 0, 1, 2, or 3 times the multiplicand, MULTA, will be introduced into the adder tree. This decoding scheme is used on the 10 least significant bits (5 least significant pairs) and is shown in Table D-1.

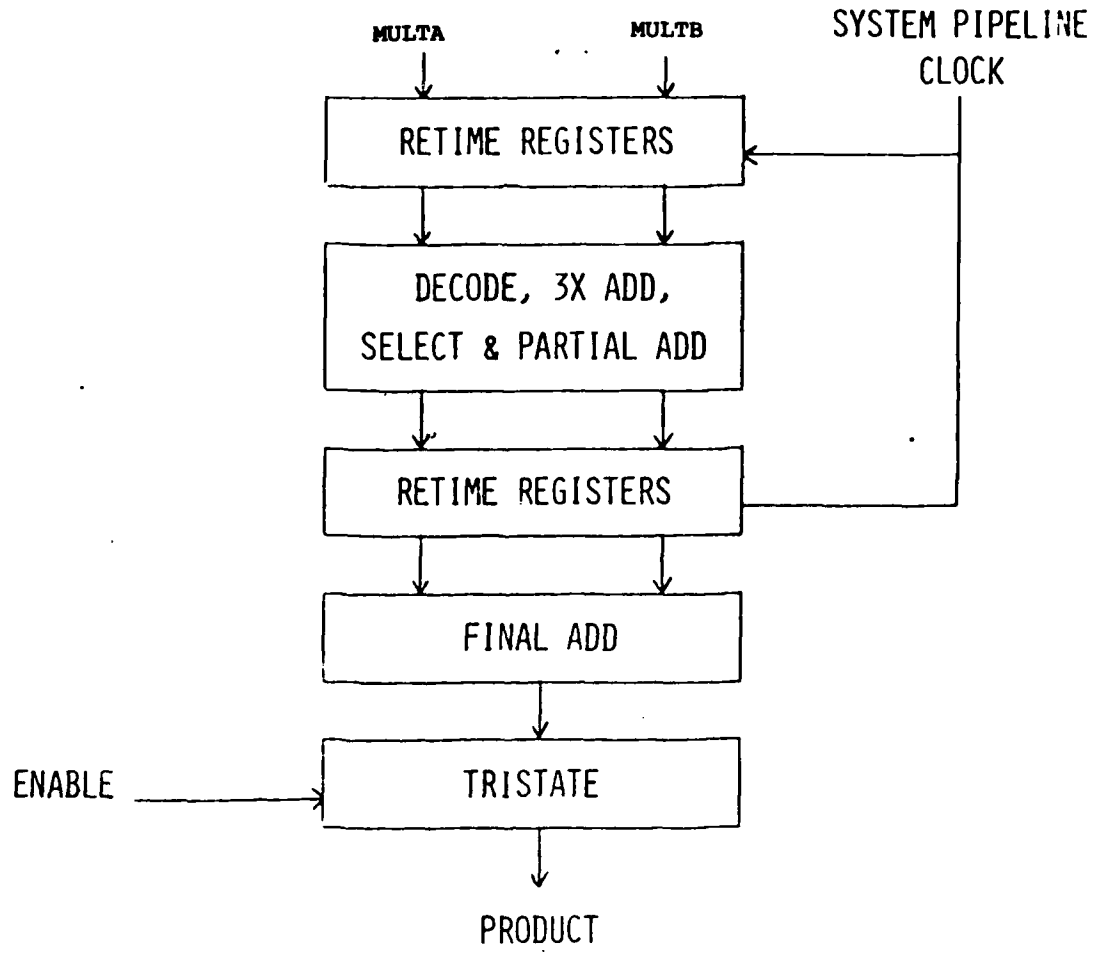


Figure D-1 12 Bit x 12 Bit Multiplier Functional Block Diagram

TABLE D-1

TCS140 MULTIPLIER DECODE AND SELECT GENERAL BIT CASE

MULTB (N)	MULTB (N+1)	Selected Input to Adders
0	0	0
0	1	MA
1	0	2MA
1	1	3MA

Special care must be taken, however, in decoding the two most significant bits. MULTB(0) and MULTB(1). Since the sign information for the word is conveyed by MULTB(0), a correction factor must be added to the product when MULTB(0) is a logic 1 when SCB indicates a negative B input word (SCB=1). The proper correction factor is -4MA. Table D-2 shows the various combinations of MULTB(0), MULTB(1) and SCB and the resultant input to the adders. Note that the -4MA term is not added directly into the adder tree. Instead, under the two conditions requiring a correction factor (MULTB (0) = 1 when SCB = 1) the -4MA term is already factored into the adder input terms, -2MA and -MA shown in Table D-2.

TABLE D-2

DECODING FOR TWO SIGNIFICANT BITS OF MULTIPLIER

MULTB (0)	MULTB (1)	SCB	Selected Input to Adders
0	0	X	0
0	1	X	MA
1	0	0	2MA
1	0	1	-2MA
1	1	0	3MA
1	1	1	-MA

For example, when MULTB(0)=1, MULTB(1)=0, and SCB=0, the normal input to the adders is 2 MA. However, when SCB=1 for the same states of MULTB(0) and MULTB(1), the correction factor of -4 MA must be added to account for the negative number expressed in the two's complement form. Since 2 MA - 4 MA = -2MA, the -2 MA term is formed by a simple 2's complement of 2 MA and added in the tree. The same reasoning persists for the last line in the table since 3 MA - 4 MA = -MA.

The MA, 2 MA and 3 MA inputs to the select gates in the decoding logic are formed from the retimed multiplicand MULTA. MA is the same as MULTA except that it is extended to 14 bits from the 12 bits of MULTA by the addition of two bits at the most significant end as shown in Fig.D-2(b). These sign extension bits, SEA, are "0" except when both MULTA(0) and SCA are "1" as shown in Table D-3. The 2 MA term is formed by shifting MULTA one place to the left, the least significant bit becoming a "0". The 2 MA term is also expanded to 14 bits by the addition of SEA at the most significant end. The 3 MA term is formed by adding the MA and 2 MA terms as shown in Fig. D-2(a). The three quantities MA, 2 MA and 3 MA are made available to each of the six select circuits shown in Fig.D-3 whose operation has been described.

TABLE D-3

SIGN EXTENSION BITS FOR MA AND 2MA

SCA	MULTA (0)	SEA
0	0	0
0	1	0
1	0	0
1	1	1

	SEA	M1A12	M1A11	M1A10	M1A9	M1A8	M1A7	M1A6	M1A5	M1A4	M1A3	M1A2	M1A1
+	M1A12	M1A11	M1A10	M1A9	M1A8	M1A7	M1A6	M1A5	M1A4	M1A3	M1A2	M1A1	
	M3A14	M3A13	M3A12	M3A11	M3A10	M3A9	M3A8	M3A7	M3A6	M3A5	M3A4	M3A3	M3A2	M3A1

a. 3 x A Adder

MA	SEA	SEA	M1A12	M1A11	M1A10	M1A9	M1A8	M1A7	M1A6	M1A5	M1A4	M1A3	M1A2	M1A1
2 MA	SEA	M1A12	M1A11	M1A10	M1A9	M1A8	M1A7	M1A6	M1A5	M1A4	M1A3	M1A2	M1A1	0
3 MA	M3A14	M3A13	M3A12	M3A11	M3A10	M3A9	M3A8	M3A7	M3A6	M3A5	M3A4	M3A3	M3A2	M3A1

b. Select Network Output Word

Fig. D-2 Formulation of 2X and 3X MULTA

The outputs of the select circuits, labeled a, b, c, d, e, and f in Fig. D-3 are the inputs to the adder tree generating the product. The term "a" is obtained from decoding the two least significant bits of MULTB, the term "b" is obtained from decoding the next two more significant bits, etc., until "f" is obtained from decoding the two most significant bits of MULTB. The adder tree is organized for maximum speed with only three levels of addition required to produce the product. A level of retiming is placed in the adder tree which provides two levels of retiming in the data path through the array.

The operation of the adders in the adder tree are detailed in Figs. D-4 through D-6. In the first level, a is added to b to obtain ab, c is added to d to obtain cd and e is added to f to obtain ef. Since the b, d, and f terms are each left shifted from the respective a, c, and e terms by two places, the a, c, and e terms are extended by sign fill. The sign fill is a "0" for unsigned and positive numbers and a "1" for negative numbers. Table D-4 gives the rules for developing the sign fill, ASF, for term a. The same procedure is used for the CSF and ESF sign fill for terms c and e.

TABLE D-4

SIGN FILL FOR THE ab ADDER

SCA	A14	ASF
0	0	0
0	1	0
1	0	0
1	1	1

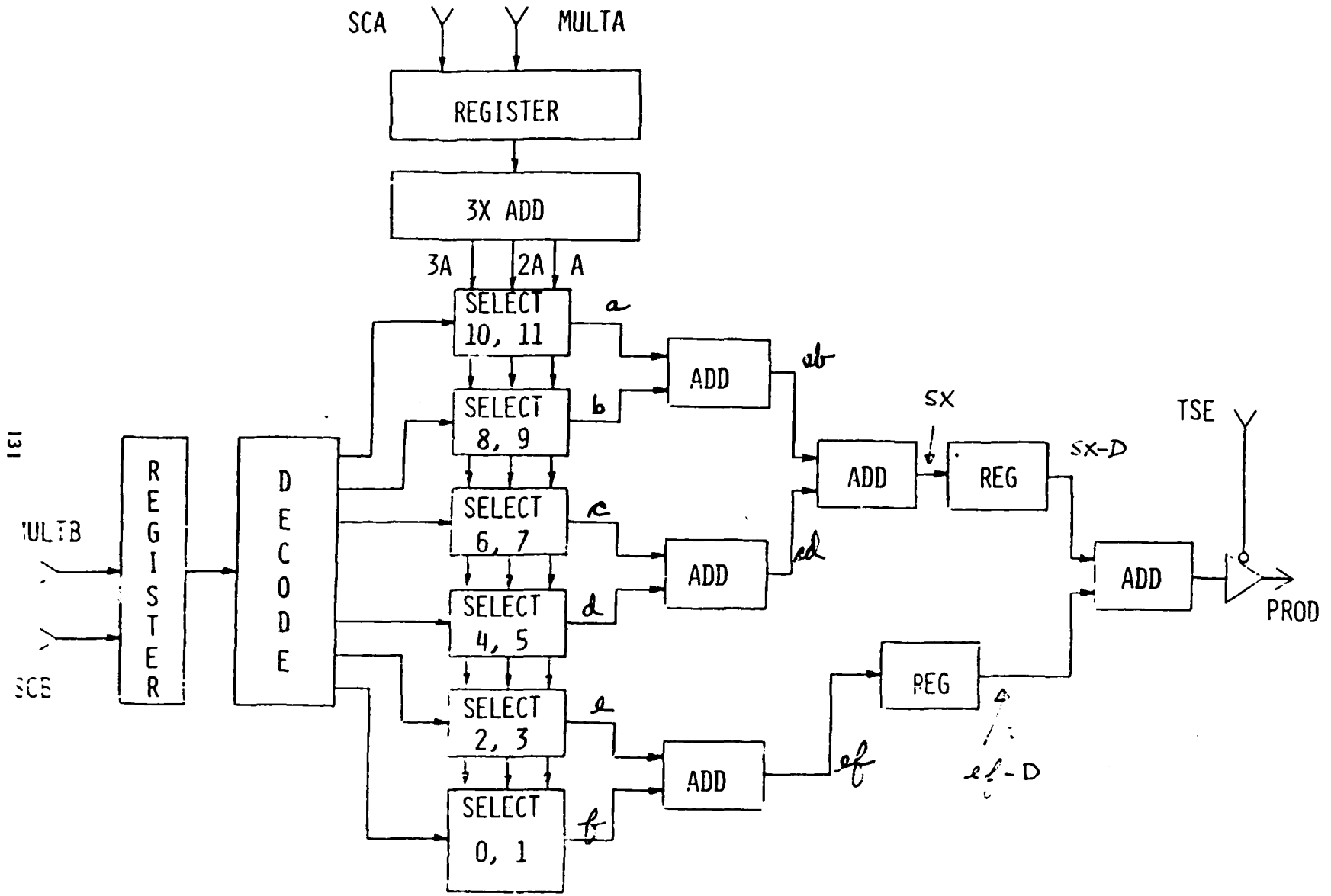


Figure D-3 TCS140 Multiplier Detailed Block Diagram

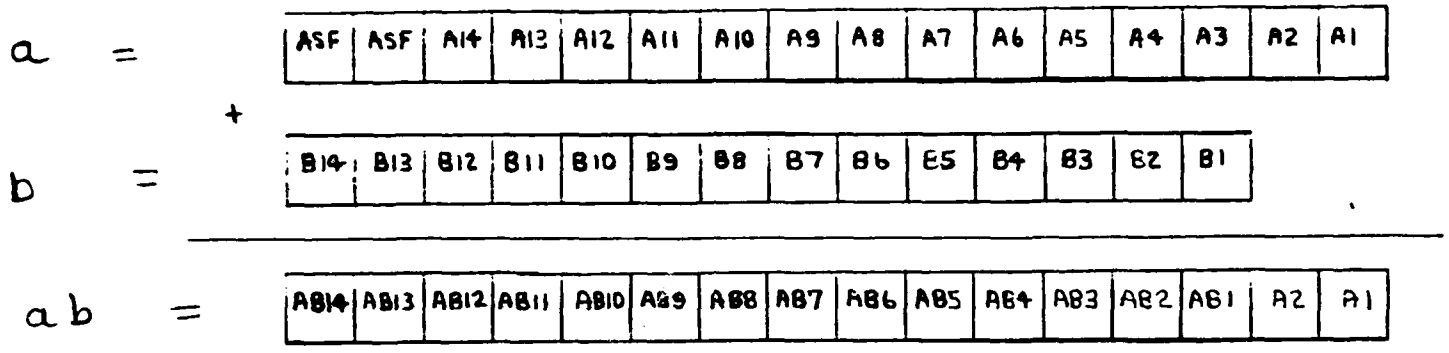
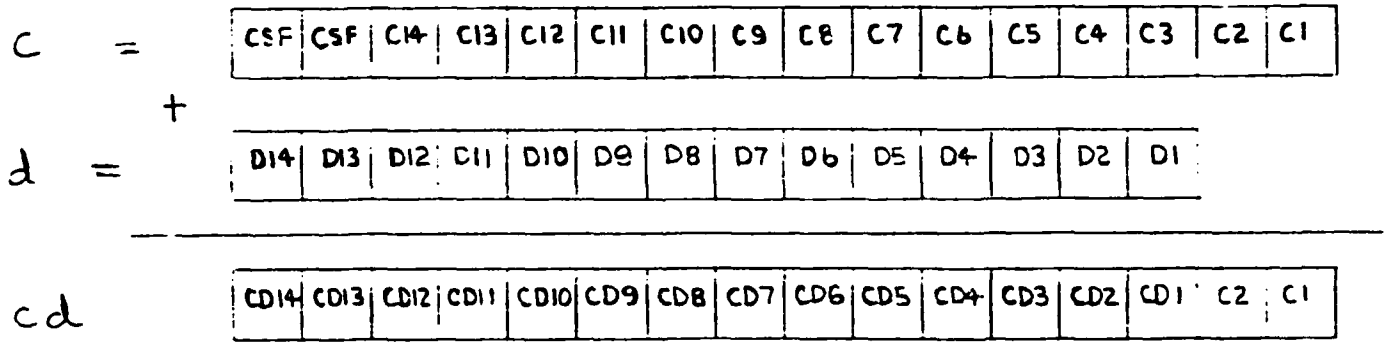


Figure D-4 (a)



Figure, D-4 (b)

Figure D-4 Multiplier Addition Tree Operation (Part 1)

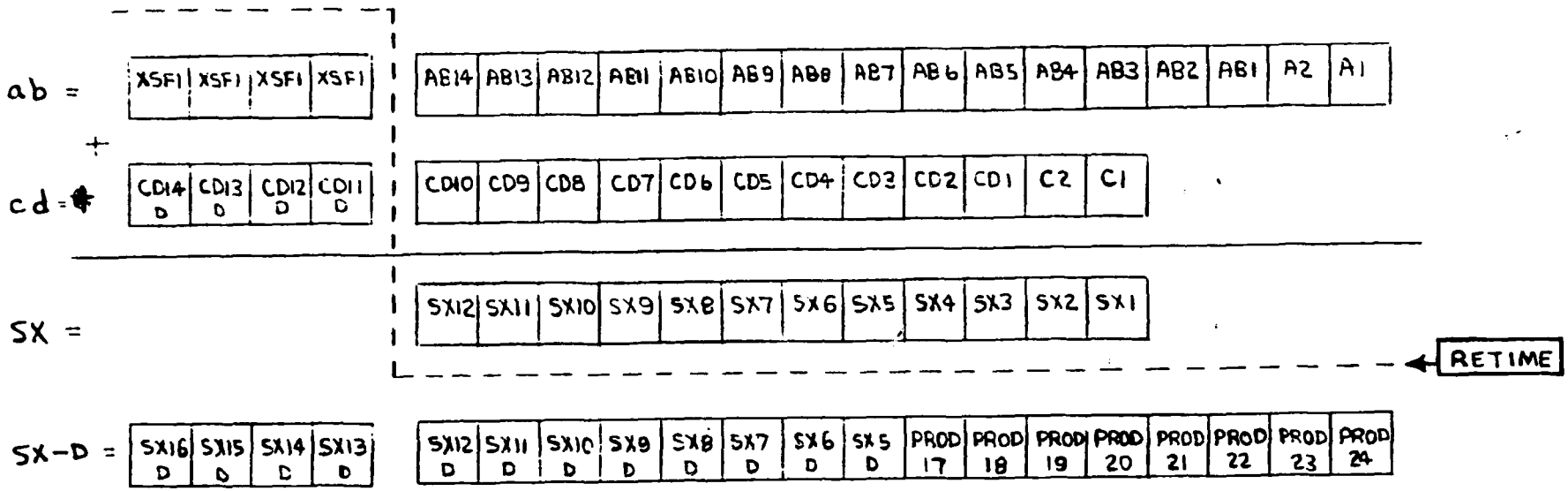


Figure D-5 Multiplier Adder Tree Operation (Part 2) (SX Adder)

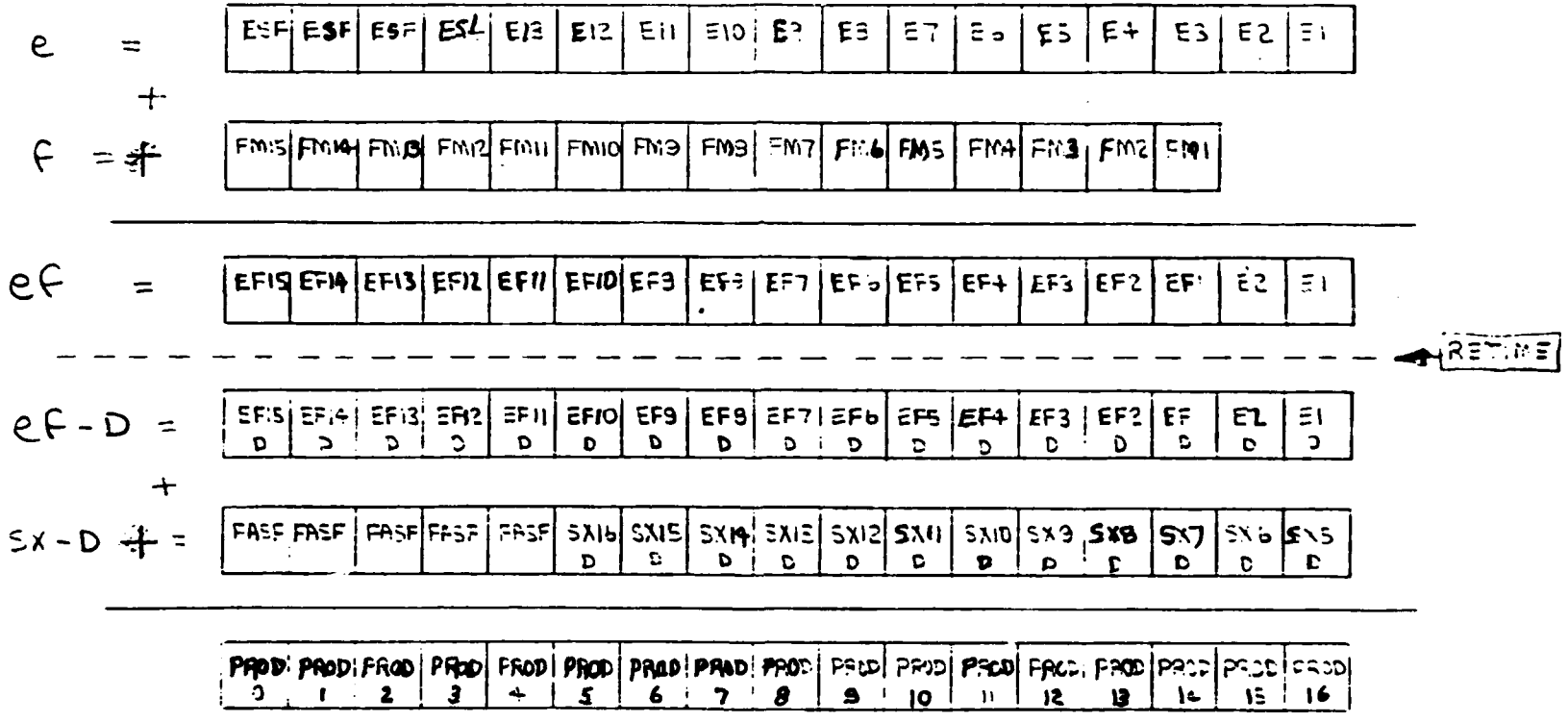


Figure D-6 Multiplier Adder Tree Operation (Part 3)

In the second level of the adder tree ab is added to cd to obtain the intermediate result sx (Fig. D-5). Since cd is left shifted from ab by four places, sign fill is used to extend the ab term. The retiming takes place in the middle of this adder, the four most significant bits of the addition occurring after retiming. The less significant bits are retimed after the sum is produced. The ef term is retimed at the second level of the adder tree with no addition required.

In the final level of the adder tree, the retimed sx and ef terms are added to form the product. The 8 least significant bits, LSBs, of the retimed sx are the 8 LSBs of the product. Once again, the sx term is extended by sign fill to match the ef term in length.

1.2 Multiplier I/O Signals

Table D-5 shows the input signals to the multiplier.

TABLE D-5

TCS140 INPUT SIGNALS

		Number of Signals
1.	V_{cc} - Power Input	1
2.	GND - Power Return	1
3.	MULTA(0) thru MULTA(11) - twelve bit binary input (MULTIPLICAND) with MULTA(0) being the MSB	12
4.	MULTB(0) thru MULTB(11) - twelve bit binary input (MULTIPLIER) with MULTB(0) being the MSB	12

TABLE D-5

TCS140 INPUT SIGNALS (Continued)

5.	SCA - sign control bit for MULTA(0 - 11) where 0 = positive input, 1 = 2's complement input	1
6.	SCB - sign control bit for MULTB(0 - 11) where 0 = positive input, 1 = 2's complement input	1
7.	CLK - register clock, rising edge trigger	1
8.	TSE - 0 enables the output, 1 is a high impedance state	1
	Total	30

The multiplier outputs represent the 25 bits of the product and are designated PROD(0) thru PROD(24). PROD(0) is the most significant bit and conveys sign information.

The total number of Input/Output signals required by the multiplier is 55.

1.3 Multiplier Circuit Cell Description

The TCS140 is implemented with 65 individual cells. These cells are uniquely defined structures separately identified and stored in computer files. Nineteen of these cells contain array level interconnects and overhead structures such as test transistors, alignment keys, and alphanumerics required to describe the array levels and numbers. Forty-six cells contain active portions of the logic and represent the number of special designs completed for the TCS140. A complete listing of all cells is shown in Table D-6, Also shown is the number of transistors (devices) for each cell.

These cells are used in various quantities to implement the logic of the TCS140. Table D-7 shows the total cell count for the array along with the total device co nt (5122). Figure D-7 is a map of the array showing the location of the various cells.

1.4 Design Specifications

The electrical design specifications for the TCS140 Multiplier are given in Tables D-8, D-9, and Figure D-8.

The array has been designed to operate over the temperature range -55°C to +125°C. The static electrical characteristics of Table 5-10 reflect current +25°C limits for the array. The majority of these parameters also reflect +125°C limits but several limits will necessitate a change for +125°C. Spe cifically, array leakage current will be changed based on measured performance in Phase 2.

The dynamic characteristics of Table D-9 are worst case numbers over the temperature range and reflect the timing waveforms of Figure D-8.

The multiplier critical path was simulated using the process and device parameters identified in Section 1.3 along with the device geometries of each cell to determine that the specified delays would be met. Device sizes and/or layouts were modified in those cases where out-of-limit results were initially obtained. The simulations of the final TCA140 configuration state that the design specifications will be achieved.

TABLE D-6

TCS140 CELL CONTENT

Cell #	Description	Derived From	# Devices
D10	Half Adder ($\bar{a}$,$\bar{b}$) 2 Inv.	---	18
D13	Half Adder (a,b)	D16	12
D15	Half Adder (a,b)	D16	12
D16	Half Adder (a,b)	---	12
D20	Adder Input Select	---	24
D21	Adder Input Select	D20	24
D22	Adder Input Select	---	24
D30	Full Adder (a,b,c)	---	28
D31	Full Adder (a,b,c)	D30	28
D32	Full Adder (a,b,c)	---	28
D33	Full Adder (a,b,c)	D36	30
D34	Full Adder (a,b,c)	D36	30
D35	Full Adder (a,b,c)	D36	30
D36	Full Adder (a,b,c)	---	30
D37	Full Adder (a,b,c)	D30	28
D38	Full Adder (a,b,c)	D32	28
D40	Full Adder (a,b,c)	---	30
D41	Full Adder (a,b,c)	D40	30
D42	Full Adder (a,b,c)	---	30
D43	Full Adder (a,b,c)	D46	28
D44	Full Adder (a,b,c)	D46	28
D45	Full Adder (a,b,c)	D46	28
D46	Full Adder (a,b,c)	---	28
D48	Full Adder (a,b,c)	D42	30
D50	Final Addend Select	---	6
D51	Final Addend Select, Inv.	---	8
D52	Final Addend Select	D50	6
D53	Final Addend Select	D50	6
D60	Retimer	---	16
D61	Retimer	---	16
D63	Retimer	D61	16
D64	Retimer	---	18
D66	Retimer	D60	16
D67	Retimer	D61	16
D70	Output Driver	---	8
D71	Output Driver	---	8
D80	Input Pad, Buffer	---	2
D81	Input Pad, Buffer	---	2
D82	TTL Input Buffer	---	8
D90	Clock Driver	---	6
D91	Sign Fill	---	18
D92	Sign Fill Registers	---	32
D93	Far Left Center Interconnect	---	0
D94	SC, SD Decode;	---	40
D95	SE, SF Decode; EN; SEB	---	60
D96	SA, SB, SC Decode; SEA	---	76
D190	Array - Lower Right	---	2
D191	Array - Upper Right	---	0
D192	Array - Mid Right	---	0
D193	Array - Center Left	---	0

TABLE D-6

TCS140 CELL CONTENT (Continued)

Cell #	Description	Derived From	# Devices
D194	Array - Left	---	0
D195	Array - Far Left	---	0
D100	TCS140	---	---
D101	Numbers	---	---
D103	PLY	---	---
D104	N+	---	---
D105	CNT	---	---
D106	MET	---	---
D108	ILD	---	---
D109	P+	---	---
D110	S&R	---	---
D111	Align Dark	---	---
D112	Align Light	---	---
D113	Test Device	---	---

TABLE D-7

TCS140 DEVICE COUNT

Cell #	Device Count	Number Of Times Used	Total Devices	Cell #	Device Count	Number of Times Used	Total Devices
10	18	2	36	52	6	1	6
13	12	1	12	53	6	1	6
15	12	1	12	60	16	16	256
16	12	1	12	61	16	13	208
20	24	12	288	63	16	20	320
21	24	16	384	64	18	12	216
22	24	14	336	66	16	2	32
30	28	6	168	67	16	1	16
31	28	6	168	70	8	8	64
32	28	7	196	71	8	17	136
33	30	6	180	80	2	12	24
34	30	1	30	81	2	13	26
35	30	5	150	82	8	2	16
36	30	8	240	90	6	1	6
37	28	2	56	91	18	1	18
38	28	1	28	92	32	1	32
40	30	5	150	93	--	1	---
41	30	7	210	94	40	1	40
42	30	6	180	95	38	1	33
43	28	7	196	96	76	1	76
44	28	1	28	190	2	1	2
45	28	6	168	191	--	1	---
46	28	8	224	192	--	1	---
48	30	1	30	193	--	1	---
50	6	12	72	194	--	1	---
51	8	1	8	195	--	1	---
							5122

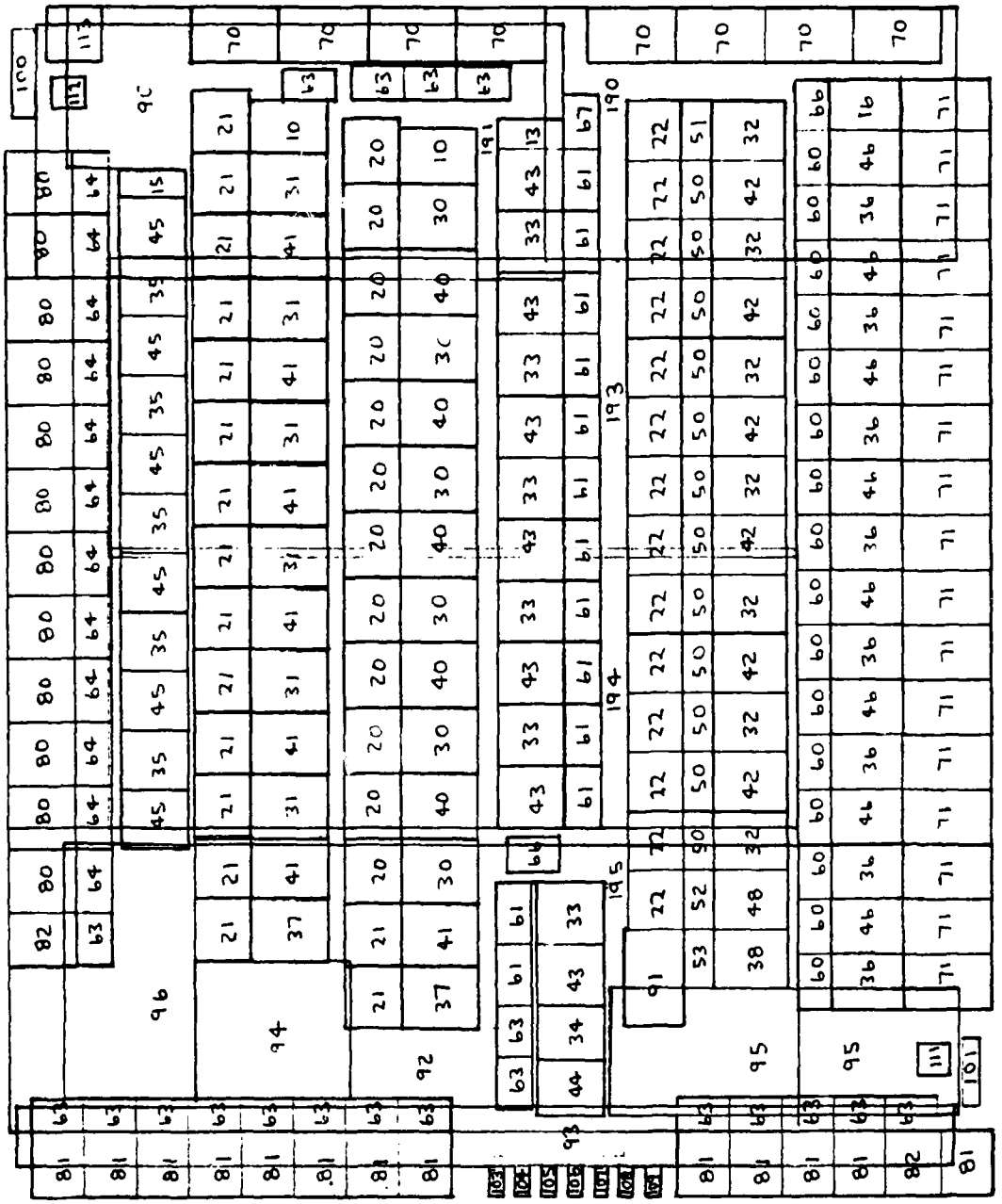


Figure D-7 Cell Map of TCS140

TABLE D-8

STATIC SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	-55°C to +125°C
Non-Operating	-65°C to +150°C
Supply Voltage	+15V nonoperating
Input Voltage	-.5V to (Vcc + .5V)

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	-	250	μamp
VOL Output Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input Low	5 10	-	1.5 3.0	1.5 3.0	Volts
VIH Input High	5 10	3.5 7.0	3.5 7.0	-	Volts
IO Output Sink and Source	5 10	-	1.5 1.5	within .5Vof Supply or GND	MA
Iin Input Current	0 < Ein < Vcc	-	.3	1	μamp
Cin data/clock	any	-	2	3/5	pf
Vcc	-	4.5	10	12	Volts

NOTES: 1. Iin for T^2L 200μA 2. Vin for T^2L: VIL 0.8V max
VIH - 2.0V min

TABLE D-9

SWITCHING CHARACTERISTICS

CHARACTERISTICS	Vcc	MIN	TYP	MAX	UNITS
Output Rise and Fall Time (15pf load)	5 10	-	30 15	40 18	nsec nsec
Data Setup Time	10	-	5	7	nsec
Data Hold Time	10	-	8	10	nsec
Clock Width	any	50	75	-	nsec
Clock Rate	5 10	 6.66	3 6.66	-	MHZ MHZ
Clock to Output	10	-	100	115	nsec
PD @6.6 MHZ	10	-	300	-	mW

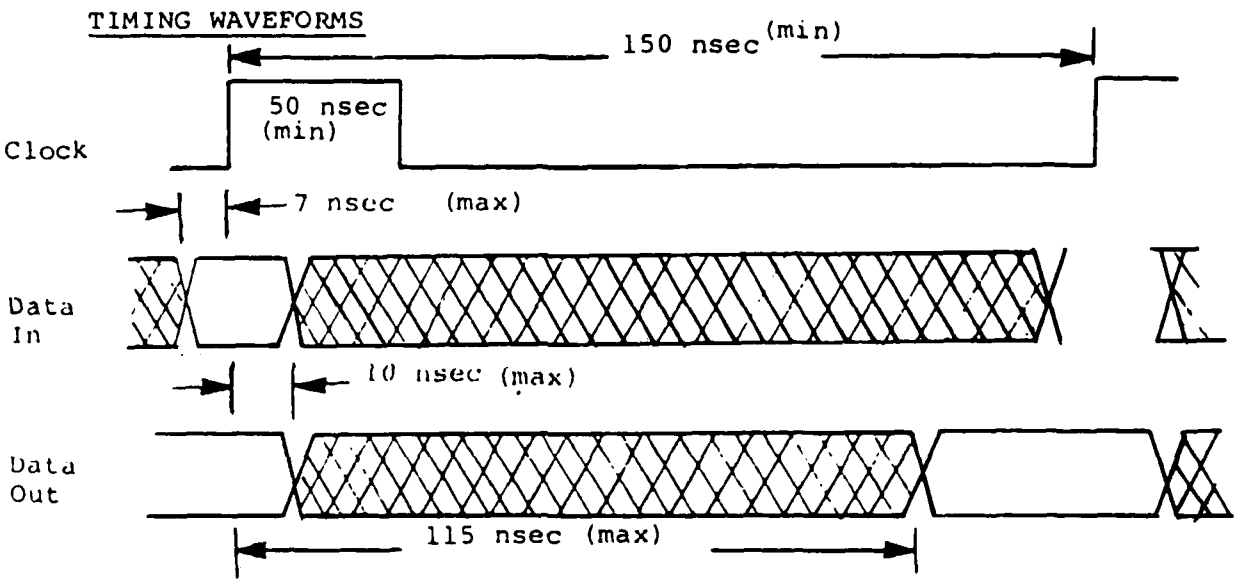


Figure D-8 Timing Waveform

1.5 Logic Verification and Test Word Generation

During the early stages of the design cycle of an array, a logic diagram is generated. Once this diagram is approved, the designer proceeds to layout the array with any mistake in the logic diagram being carried over into the array layout. The thorough checking of this diagram is therefore crucial. A TESTGEN computer simulation of the TCS140 array at the logic gate level was the method used to check the logic diagram on which the TCS140 was based. Once the logic diagram and TESTGEN computer model were approved as correct, a test pattern was generated using the verified computer model.

The method for generating the computer model was as follows. First a TESTGEN model of each cell that appears on the logic diagram is generated. These models are called macros. They are basically interconnection lists of simple gates; ANDs, NANDs, inverters; to form more complex logic structures; adders, multiplexers, shifters. Next an interconnection list of these cells as they appear on the logic diagram is generated by the designer. The information in this list plus the macro cell model definitions form a complete description of the array logic. The MACRO program converts this information into a new TESTGEN model of the array which is of the same format as the cell definitions.

This model is then checked using the TESTGEN simulation program. A total of 248 input combinations were simulated with the resultant outputs checked against the known correct multiplier outputs. When, after several corrections had been made to the logic diagram, the simulation outputs were verified as being correct, the logic diagram could be confidently approved.

The input to, and output from, this final simulation is also the test pattern that will be used to test the TCS140 processed parts. The test pattern is 248 words by 57 bits and tests 98% of all possible circuit faults. The input combinations are the ones suggested by Raytheon and are as follows:

Case 1

Both inputs treated as unsigned positive (SCA, SCB = 00).

1. All zeros x all 0's.
2. All 1's x all 1's.
3. Walking one bits across field i.e.

   0001 x 0001

   0002 x 0002

   0004 x 0004

   0010 x 0010 etc.
4. Zero x all 1's (two cases).

Case 2

Both signed (SCA, SCB = 11).

1. Same tests as in case 1 (include 4000 x 4000).
2. Negative walking zero i.e.

   7776 x 7776

   7775 x 7775

   7773 x 7773

   7767 x 7767 etc.

3. Positive ones x negative zeros i.e.

0001 x 7776

0002 x 7775

0004 x 7773

0010 x 7767 etc.

Note: reverse A and B inputs and repeat

Case 3

One input unsigned x one input two's complement (SCA, SCB = 1/0 (a), 0/1 (b). The following tests shall be performed twice (for SCA, SCB = 0, 1 and SCA, SCB = 1, 0).

1. Case 1 Tests #1, #2, #4.
2. Case 2 Test #3.

1.6 Physical Characteristics

Figure D-9 shows a checkplot of level 6 of the final TCS140 layout. The saw-like structures around the periphery of the array are part of the high voltage static discharge protection circuitry employed on all array inputs.

The array is 190 mils x 233 mils in size and contains 5122 devices. This results in a size factor of 8.6 sq. mils per device. This number is based on the border-to-border dimensions and includes all overhead such as pads, descriptive alphanumerics, and test transistors. This size factor is considered excellent for non-memory arrays using current layout design rules.

The 55 active pins for the TCS140 require the array to be packaged in a 64 lead package. Two packages will be used in Phase 2. One is a 64 lead dual-in-line ceramic (DIC) and the second is a 64 pin hermetic chip carrier (HCC). The latter is one of a series of similar leadless packages being developed under Air Force Materials Laboratory sponsorship by RCA.

Figure D-10 is a bonding diagram for the array showing relative positions of pads on the array as well as specific package pin numbers. Pinout information is also shown in Table D-10.

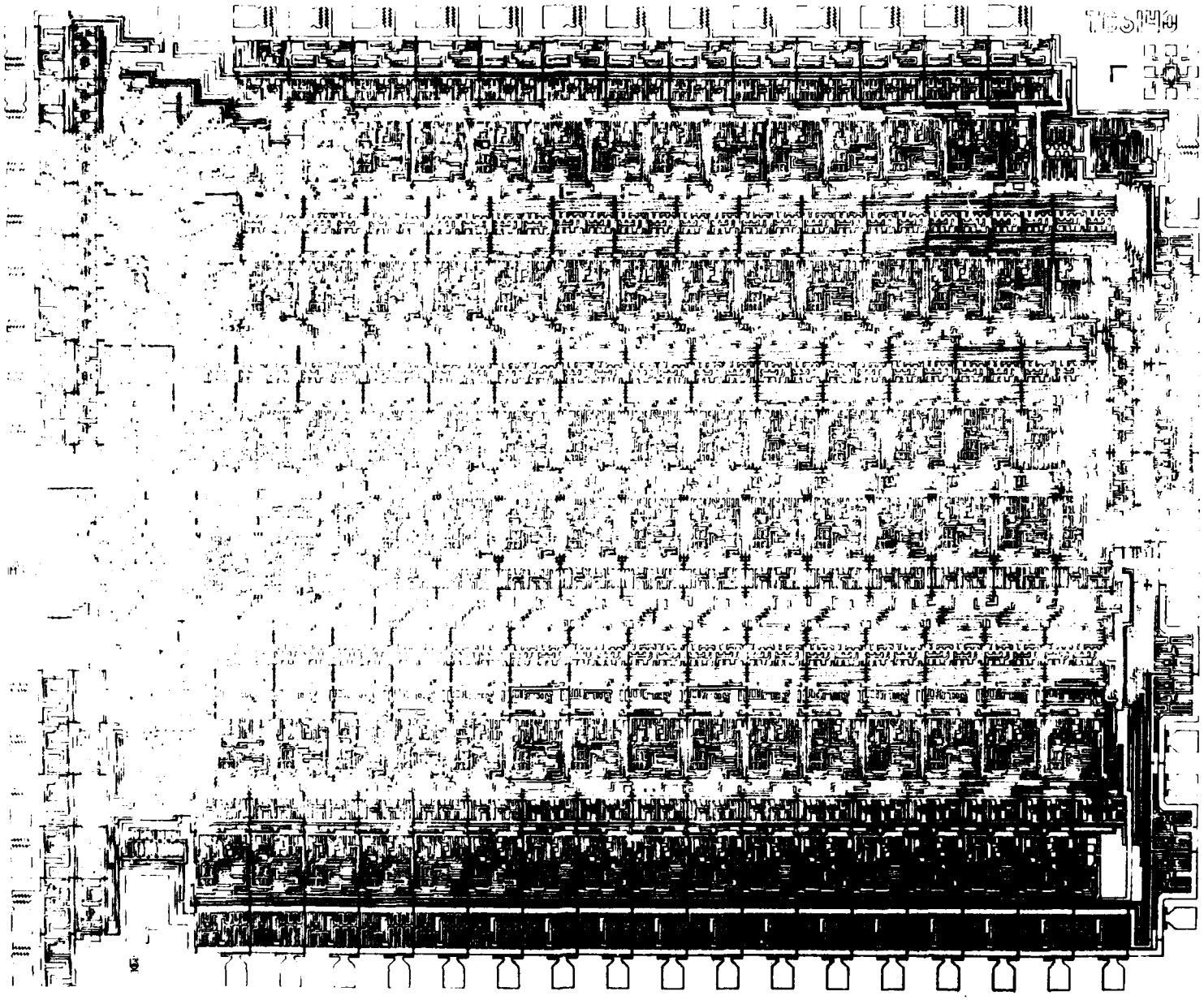


Figure D-9 TCS140 Multiplier Metal Layer Checkplot

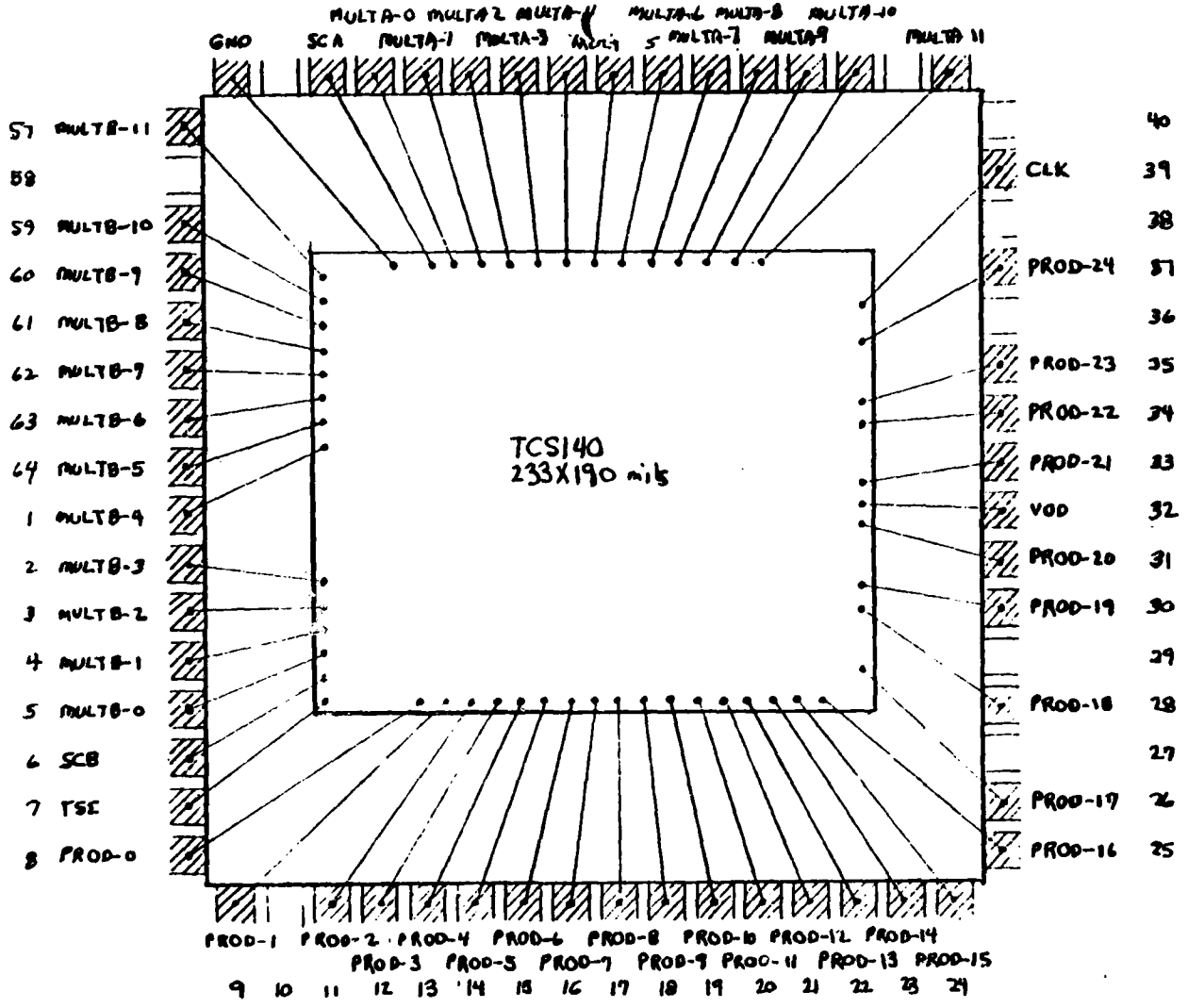


Figure D-10 TCS Bonding Diagram

TABLE 10

TCS140 PIN CONNECTIONS

Pin #	Signal Name	Pin #	Signal Name
1	MULTB-4	33	PROD-21
2	MULTB-3	34	PROD-22
3	MULTB-2	35	PROD-23
4	MULTB-1	36	NC
5	MULTB-0	37	PROD-24
6	SCB	38	NC
7	TSE	39	CLK
8	PROD-0	40	NC
9	PROD-1	41	MULTA-11
10	NC	42	NC
11	PROD-2	43	MULTA-10
12	PROD-3	44	MULTA-9
13	PROD-4	45	MULTA-8
14	PROD-5	46	MULTA-7
15	PROD-6	47	MULTA-6
16	PROD-7	48	MULTA-5
17	PROD-8	49	MULTA-4
18	PROD-9	50	MULTA-3
19	PROD-10	51	MULTA-2
20	PROD-11	52	MULTA-1
21	PROD-12	53	MULTA-0
22	PROD-13	54	SCA
23	PROD-14	55	NC
24	PROD-15	56	GND
25	PROD-16	57	MULTB-11
26	PROD-17	58	NC
27	NC	59	MULTB-10
28	PROD-18	60	MULTB-9
29	NC	61	MULTB-8
30	PROD-19	62	MULTB-7
31	PROD-20	63	MULTB-6
32	VDD	64	MULTB-5

APPENDIX E
TCS142 DESCRIPTION

1.0 Detailed Description of TCS142

1.1 Functional Description

The TCS142 Multiport/FIFO array, Fig. E-1, serves a dual role in the Microsignal Processor. By external selection the array functions either as a multiport random access memory (RAM) or as a first-in-first-out memory (FIFO).

A generalized block diagram of the TCS142 is seen in Fig. E-2, and shows how this selection is done. When the FIFO select signal, FSL, is ONE, the FIFO mode of operation is selected and the A address and write address are generated by the FIFO control logic. When FSL = 0, the Multiport mode of operation is selected, and the A address and write address are generated external to the array. Both the Multiport and FIFO mode of operation will be discussed in detail in the following paragraphs.

1.1.1 Multiport Operation

The TCS142 when configured as a Multiport (Fig. E-3), is a 16 word by 12 bit, dual port read single port write word organized random access memory. Data from the memory read ports are buffered by latches and tristates. Addresses to the memory are buffered by retimers (not shown) triggered on the positive clock edge. The memory access time, from clock going high to the leading edge of data out of the tristate buffer, is estimated to be 75 ns.

The heart of the Multiport is the memory cell described in Section 1.2. It uses a conservative design approach yet it is extremely dense. These cells are arranged into sixteen 12 bit words. Each address points to a memory word.

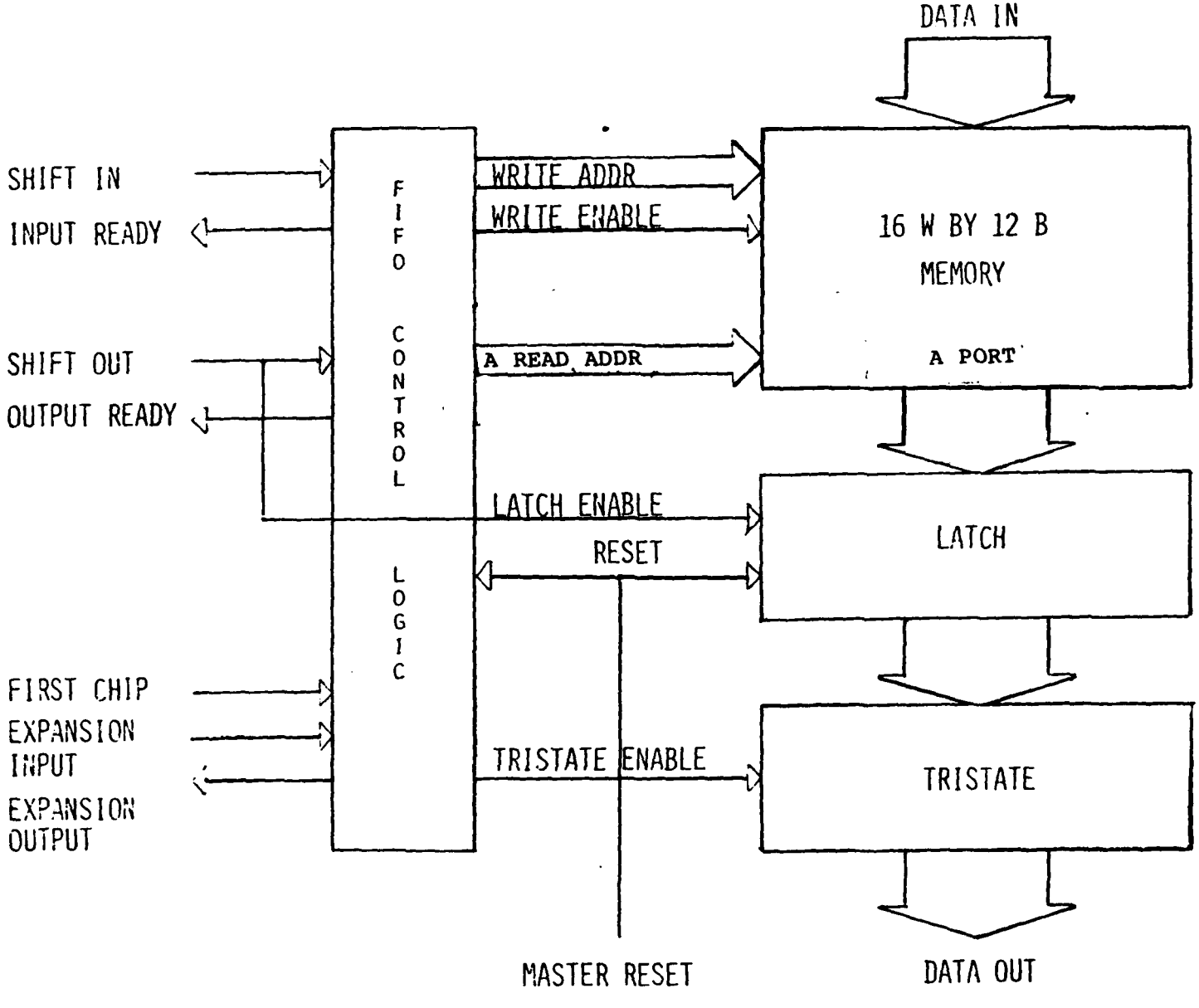


Figure E-1 TCS142 Configured as a FIFO

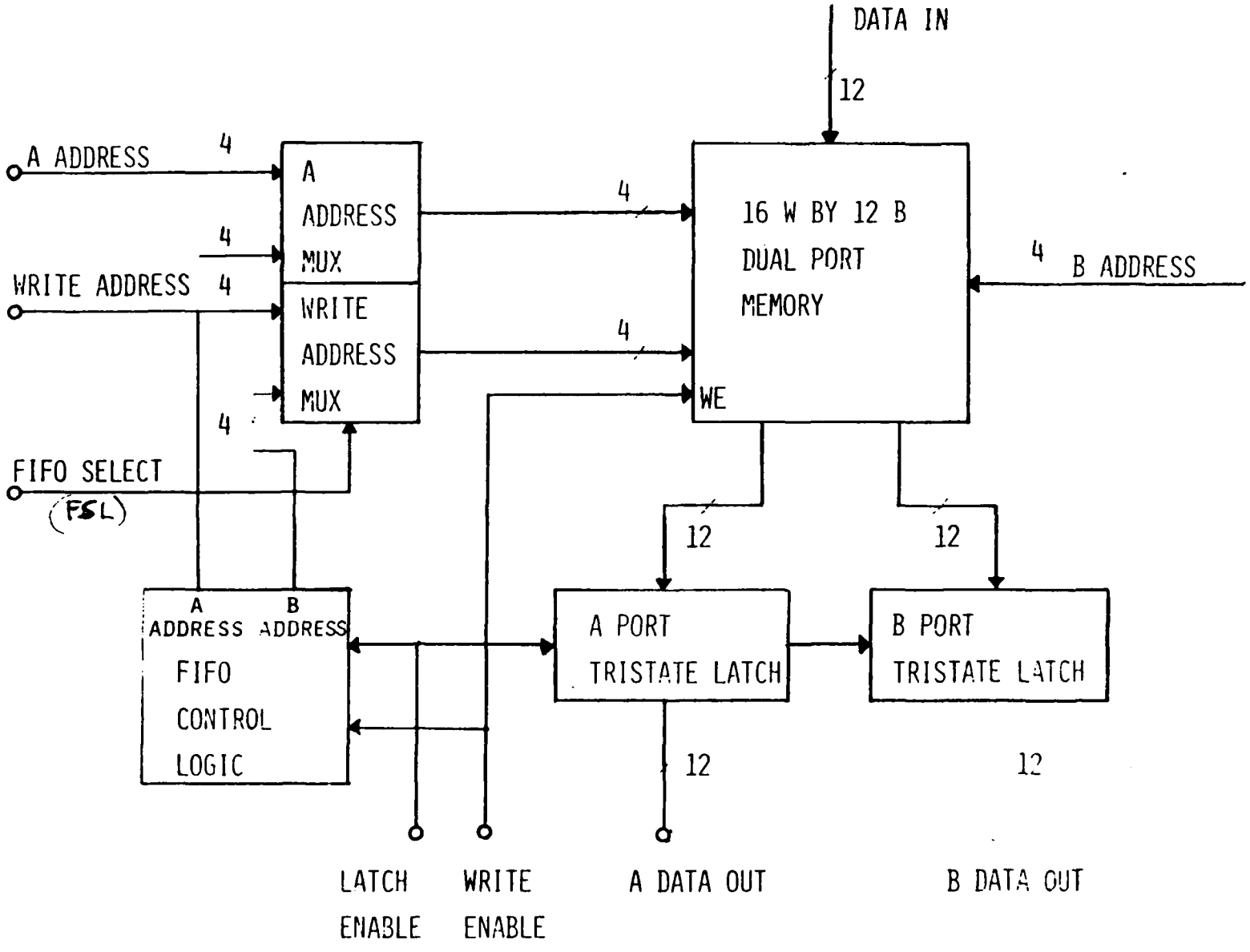


Figure E-2 TCS140 Multiport FIFO Block Diagram

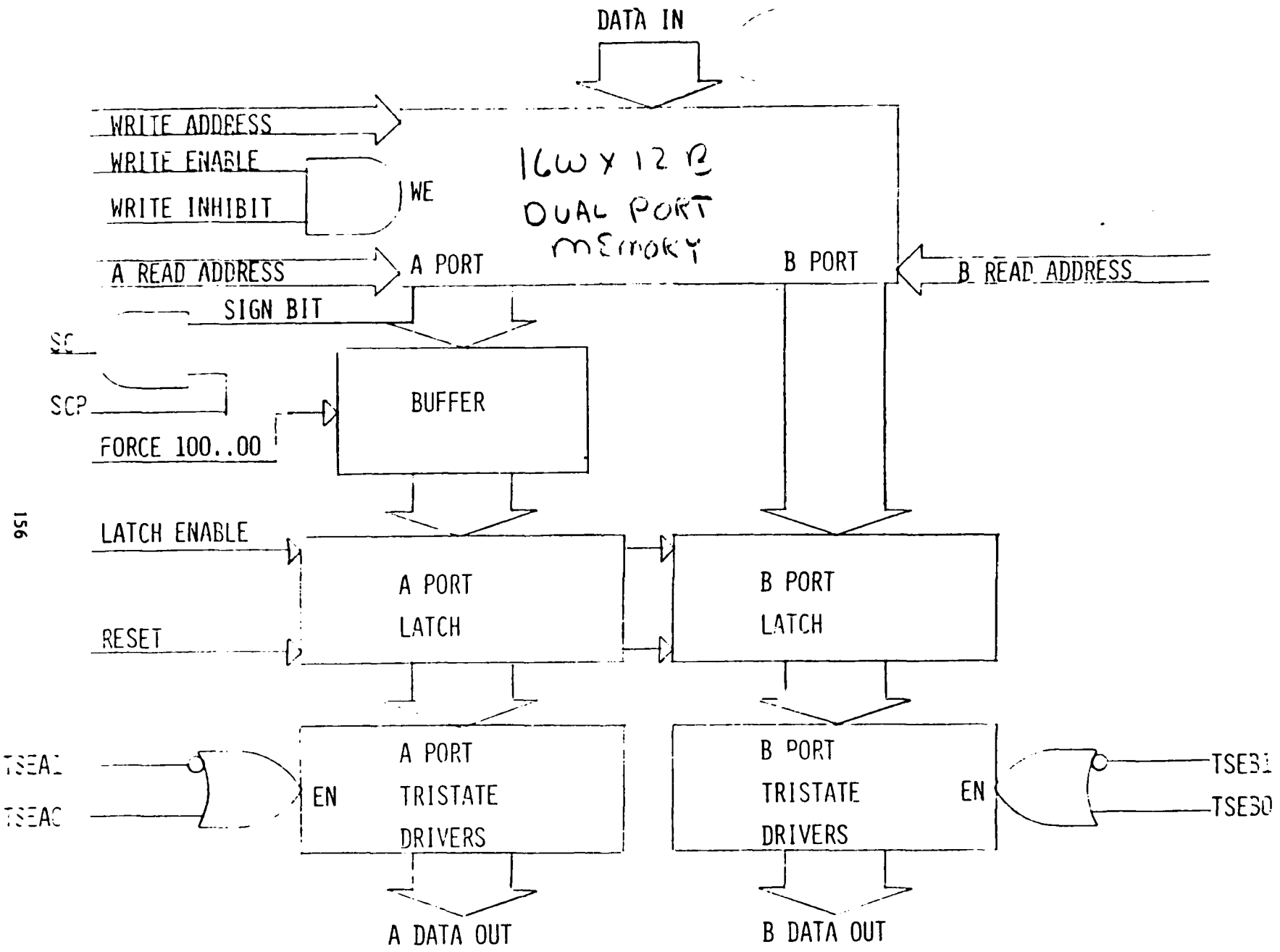


Figure E-3 TCS142 Configured as a Multiport

An address input word is retimed at the input of the array on the positive edge of clock. It is then converted, by the decode logic in the 16 word by 12 bit memory, from a 4 bit address to a 1 out of 16 bit pointer. A memory word is written into when the write address points to it and WE = 1. A memory word is dumped to the A port when the A address points to that word; likewise for the B port. Both ports are buffered by latches and tristates.

There is a master slave relation between the memory and the memory latch, the memory being the master and the latch being the slave. The latches are transparent when Latch Enable is 1 and hold their current value when latch Enable is 0. The latch can be asynchronously cleared to 0 by a zero Reset pulse.

The tristate output drivers allow expansion of the Multiport memory so that more than sixteen 12 bit words can be stored. This is done by connecting common data inputs and outputs of several different chips together. Only the outputs of the chip being read from will have their tristates enabled. These enabled tristates act as noninverting buffers while all the disabled tristates are in a high impedance state. The A port tristates are enabled or disabled depending on the state of the retimed TSEA1 and TSEA0 signals. Similarly, the B port tristates are controlled by the retimed TSEB1 and TSEB0 signals. Retiming is done on the positive clock edge. Expansion of writing into the Multiport is done by inhibiting writing into all arrays but the array to be written into by setting their Write Inhibit signals to zero.

1.1.2 FIFO OPERATION

A FIFO (First-In-First-Out) is a data buffer in which data is shifted out in the same chronological order as it was shifted in; shifting in and shifting out operation's typically being asynchonous. The main function of a FIFO is as a data buffer between two asynchronous devices. The TCS 142 in the FIFO mode is a 16-word by 12-bit FIFO with shift in and shift out rates of 6.6MHZ.

In the FIFO mode the A Read Address and Write Address are generated by the FIFO control logic converting the 16-bit by 12-word memory into a FIFO. Only the A part of the memory is used, the latches and tristates buffering this part operating as in the multiport mode.

The Input Ready signal (IR) and Output Ready signal (OR) indicate the FIFO's status (is FIFO either full or empty?). The FIFO is fully expandable by a new method for which a disclosure has been made by RCA.

The 16 word bit memory is converted to a FIFO as follows. Fig. E-4 show a block diagram of the FIFO control logic to be discussed. Figs. E-5 and E-6 give example timing diagram of the FIFO operation.

Data is shifted into FIFO as follows. Referring to Fig. E-4 when the write enable, WE, signal goes high, the data word pointed to by the Write Address Latch, (1), is written into. Also the write counter output, SICNT, is incremented (2). When WE goes low, the Write Address latch is transparent and increments to the new SICNT. In this way the FIFO writes data to successive memory locations on each WE pulse. Note that memory location 0, the first, follows 15, and last, making a closed loop of successive locations.

Data is shifted out of the FIFO in the same order as it is shifted in. When the Latch Enable, LE, goes high and data word pointed to by the Read Latch, (4) is then read out. Also the Read Counter output, SOCNT, is incremented (5). When LE goes low, the A Read Address Latch is transparent and increments to the new SOCNT. In this way the FIFO reads data from successive memory locations in the same order it was read in. The 16 word x 12 bit memory has been converted to a FIFO.

The comparator, (6), determines whether the FIFO is full or empty. If it is full, then F=0 If it is empty, then E=0. The Output Ready signal, OR, is low when either a shift out operation is in progress (LE=1) or when the FIFO is empty (E=0), otherwise it is high. The Input Ready signal, IR, is low when either a shift is in progress (WE=1) or when the FIFO is full (F=0), otherwise it is high.

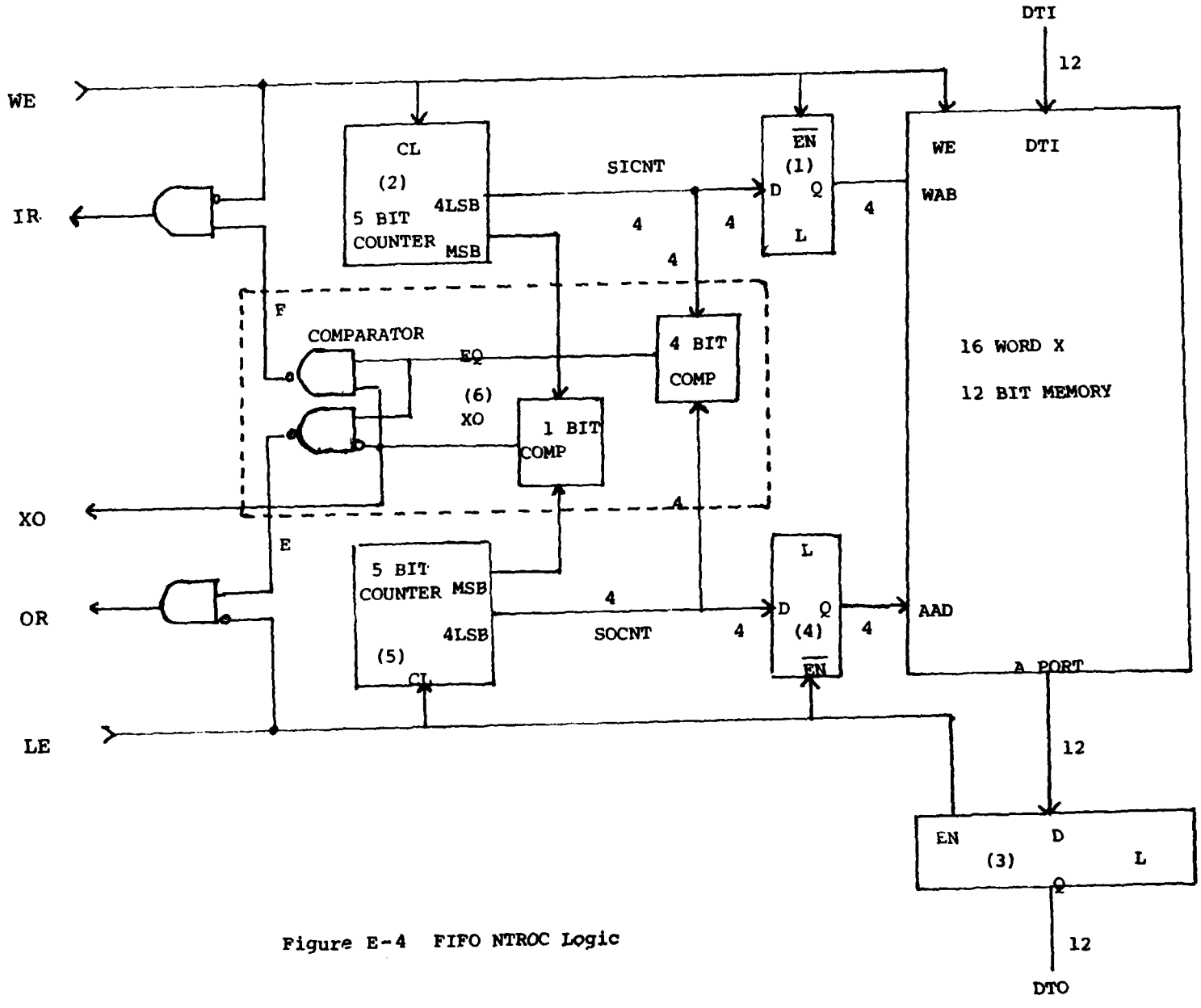


Figure E-4 FIFO NTROC Logic

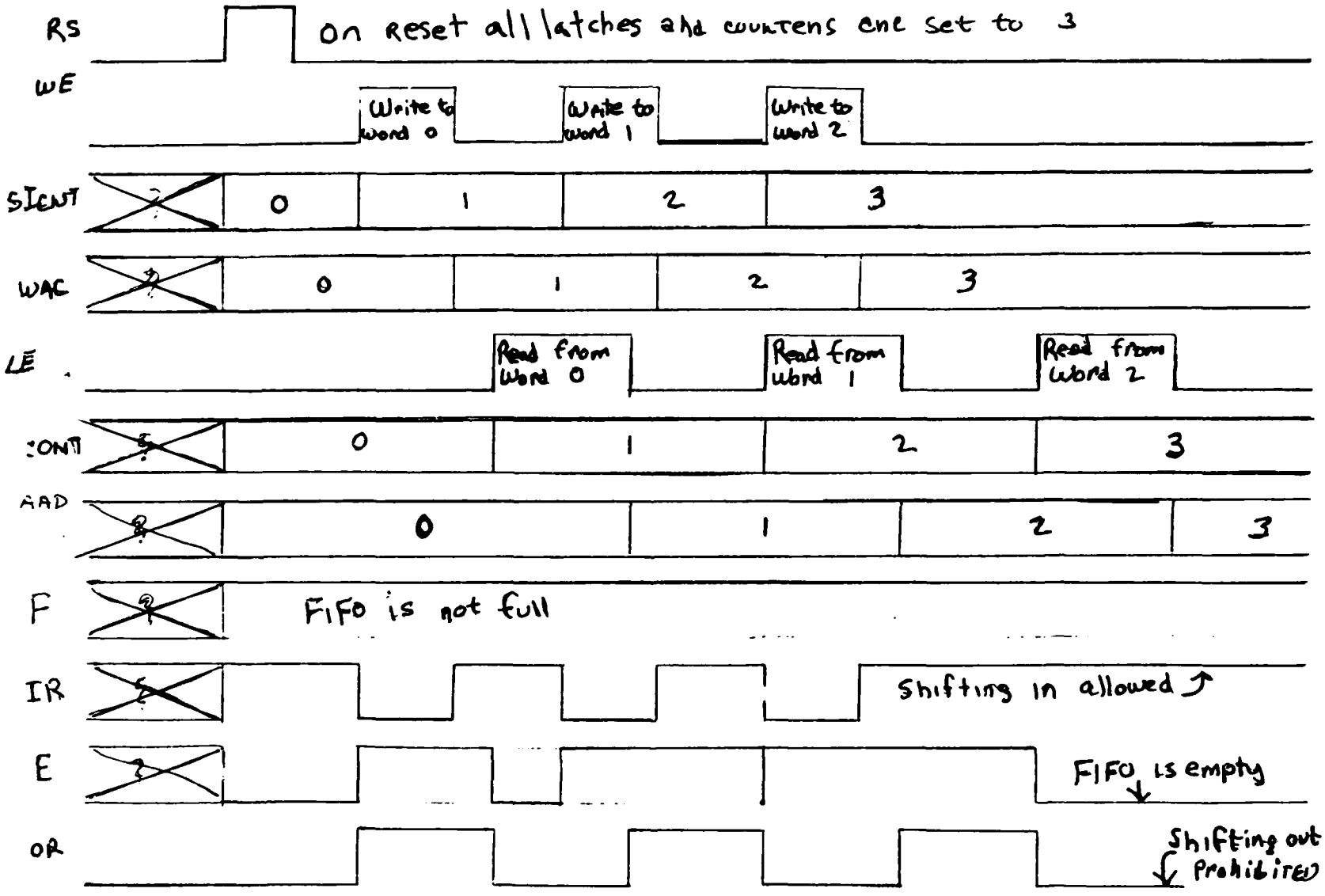


Figure E-5

FIFO TIMING DIAGRAM ILLUSTRATING NEAR EMPTY CONDITION

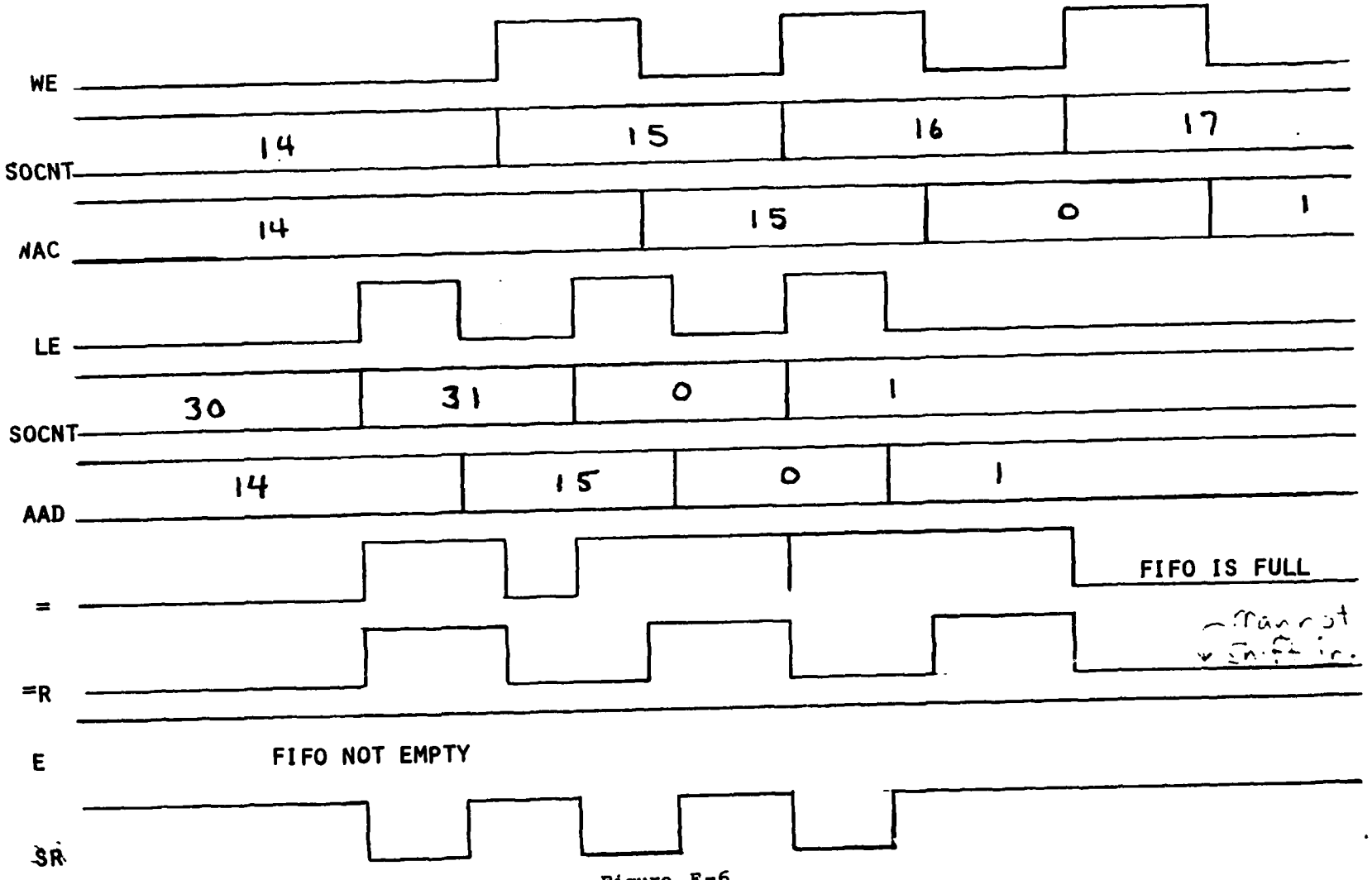


Figure E-6

FIFO TIMING DIAGRAM ILLUSTRATING NEAR FULL CONDITON AND COUNTERS ROLLOVER

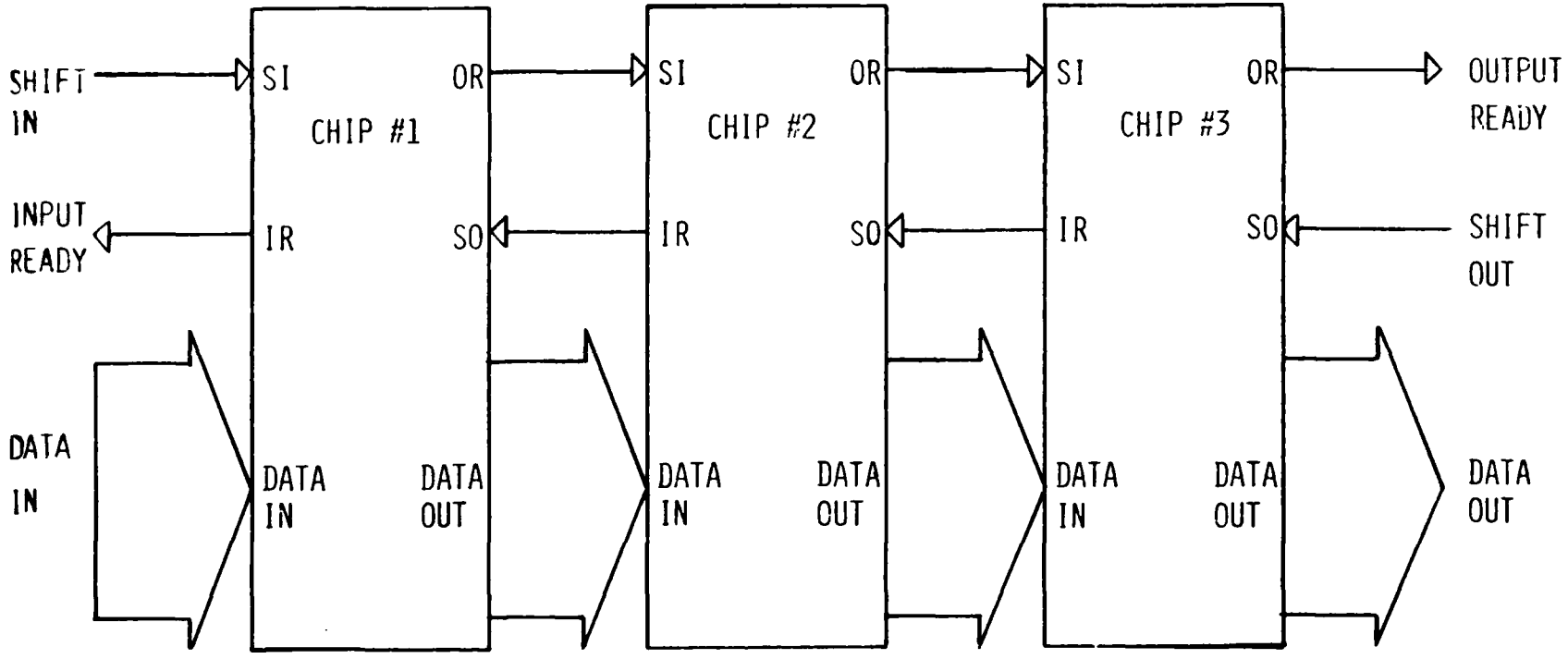


Figure E-7 Serially Expandable FIFO

The originally conceived FIFO expansion method was to expand serially (Fig. E-7). Data was shifted into the first chip in the FIFO chain and then had to ripple to the last chip before the data was available to be shifted out. Rippling of data from one FIFO to the next was to be controlled by one shot multivibrators which are difficult to fabricate on an LSI array. Also the time from data being shifted in until that same data is available to be shifted out is proportional to the length of the FIFO chain and represents a problem for high speed systems.

A method having neither of these drawbacks is to expand the FIFO in a parallel fashion (Fig. E-8). When SI goes high, data on the Input bus is shifted into the chip selected by the FIFO control logic. Similarly, when SO goes high, data is shifted to the output bus from the FIFO selected for shift out. Since access to data is direct, no rippling of data occurs and speed is independent of FIFO length. Two pins, XI and XO, determine which FIFO is selected for shift-out and which is selected for shift in. An additional pin, FC, determines which chip will be the first chip to be shifted into and, subsequently, out from, when the FIFO is reset to its initial state.

In the expanded mode, the memory locations are still shifted into and shifted out from in a successive closed loop fashion. The direction of this loop is illustrated in Fig. E-9. This shows that the next memory location after location 15 of one chip is location 0 of the next chip. This is simply a generalization of the single chip case where the next chip is the current chip.

A simplified block diagram of the logic that selects a FIFO for shift out or shift in is seen in Fig. E-10. When a chip is selected for shift-in, its Write Enable signal, WE, is the only one that follows the SI pulse. Also,

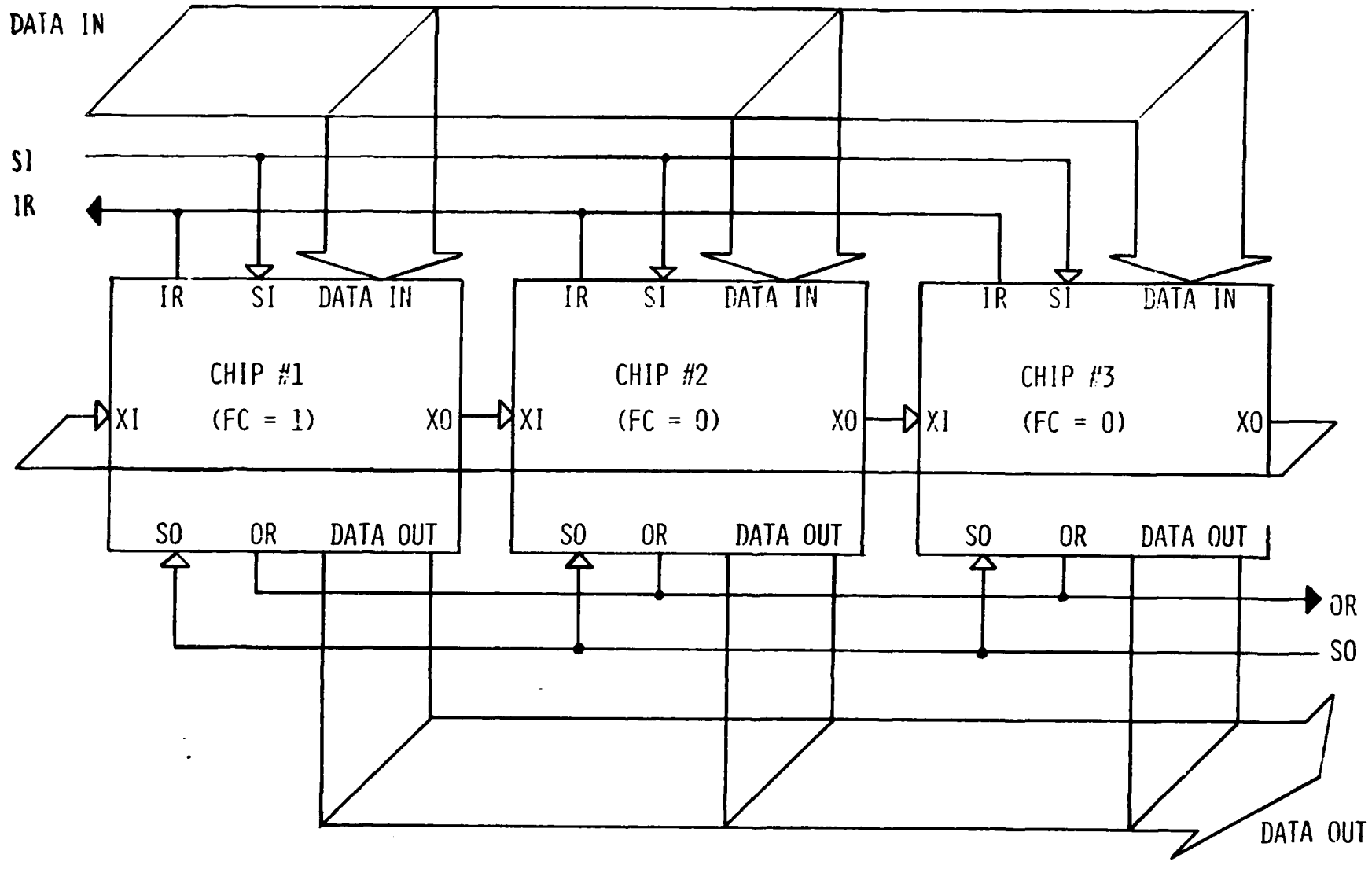


Figure E-8 Parallel Expandable FIFO

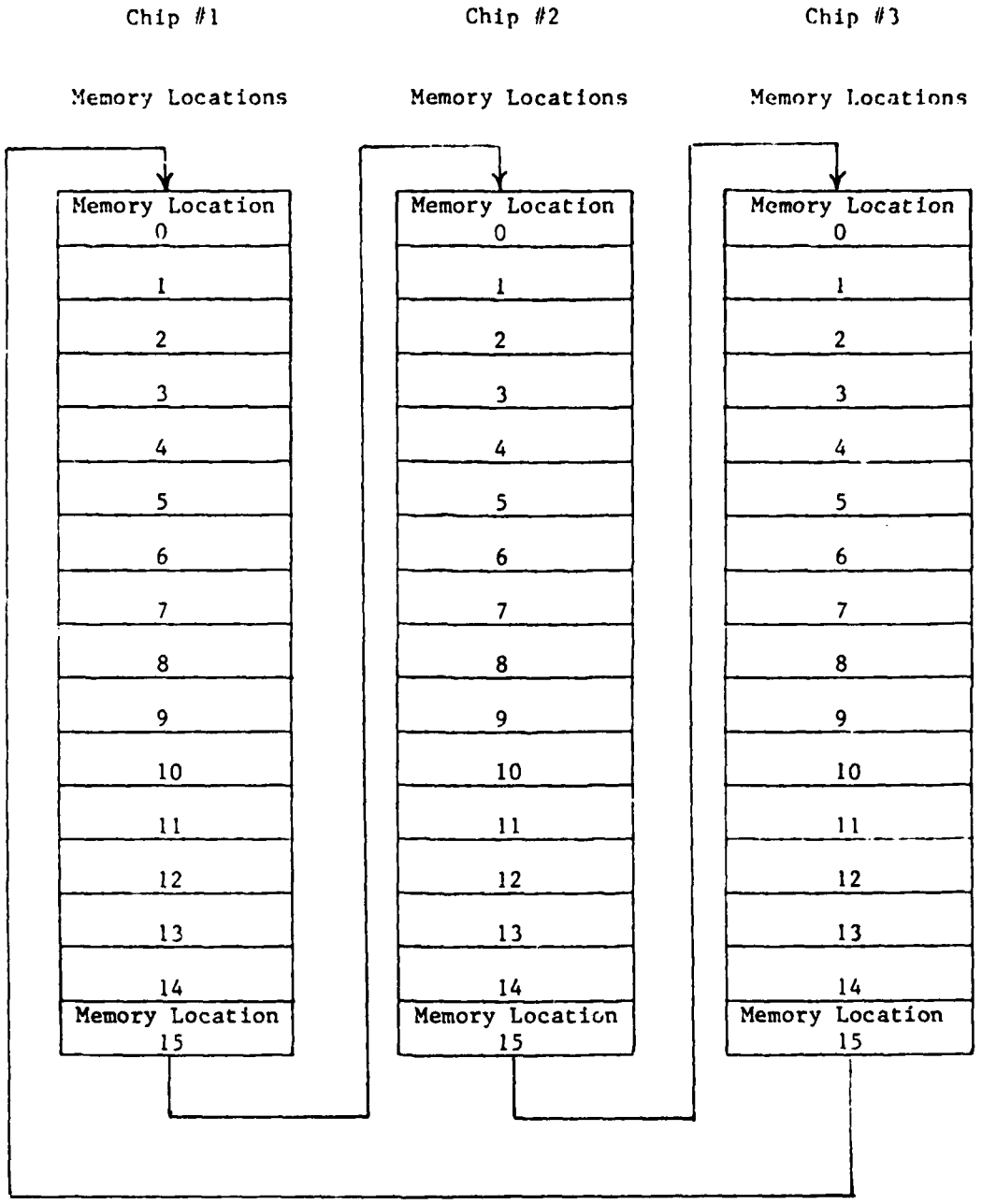


Figure E-9 Closed Loop of Successive Memory Locations

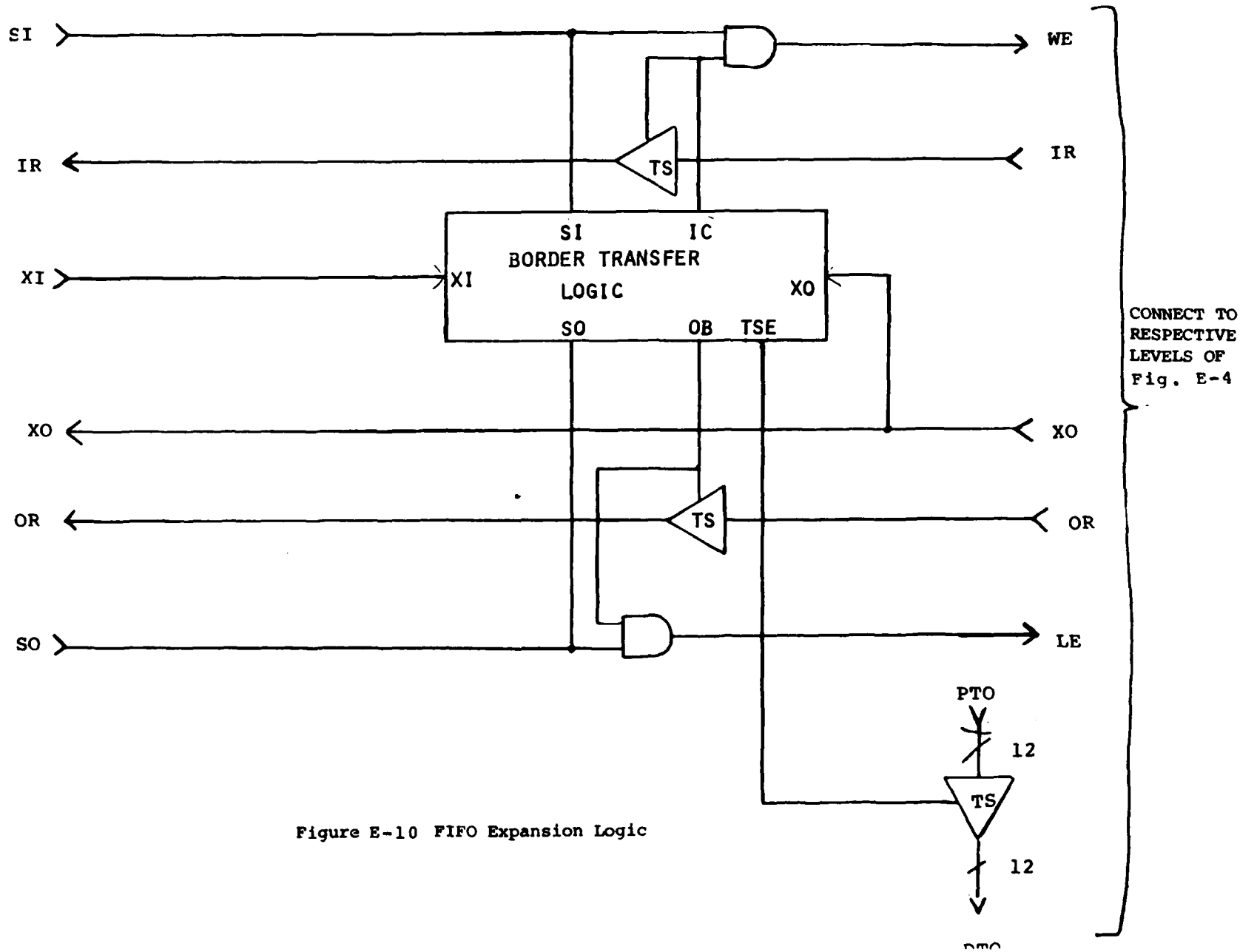


Figure E-10 FIFO Expansion Logic

only its IR tristate is enabled. This means only its counters are clocked, only its memory is written to, and it produces the IR signal. When a chip is selected for shift out, its **Latch Enable,** LE, is the only one that follows the SO pulse. Also, only its memory data tristates and OR tristate are enabled. This makes this chip the one read from and the one that generates the OR signal.

The Border Transfer Logic controls this selection of chips. The most important inputs to this logic are the XI (expansion input) and XO (expansion output). The XO signal of a chip is high when data has been shifted into memory location 15, the last, and has not yet been shifted out. The XI signal comes from XO signal of the preceding FIFO in the FIFO chain.

These two signals give enough information to determine when the transfer of shift-in control or shift-out control should occur. When XO of a chip goes high, data is being written into memory location 15 of the current chip. The next SI should write data to memory location 0 of the next chip in the chain. When XO goes low, data is being shifted out of memory location 15 of the current chip and the next SO should read data from **memory location**0 of the next. Since XO of a chip goes to both its Border Transfer Logic and the next chip's Border Transfer Logic, it contains enough information to dictate the transfer of control from one chip to the next.

The outputs of the Border Transfer Logic are IB, OB, and TSEA. IB controls shift-in operation by enabling **the Write Enable** signal to follow SI. It is also the Tristate control of the IR. Shift-out operations are controlled by OB and TSEA. OB controls the enabling of the latch enable signal and also the OR tristate. The TSEA signal controls the enabling of the memory data tristates. Timing diagrams for these signals are shown in **Fig. E-11.**

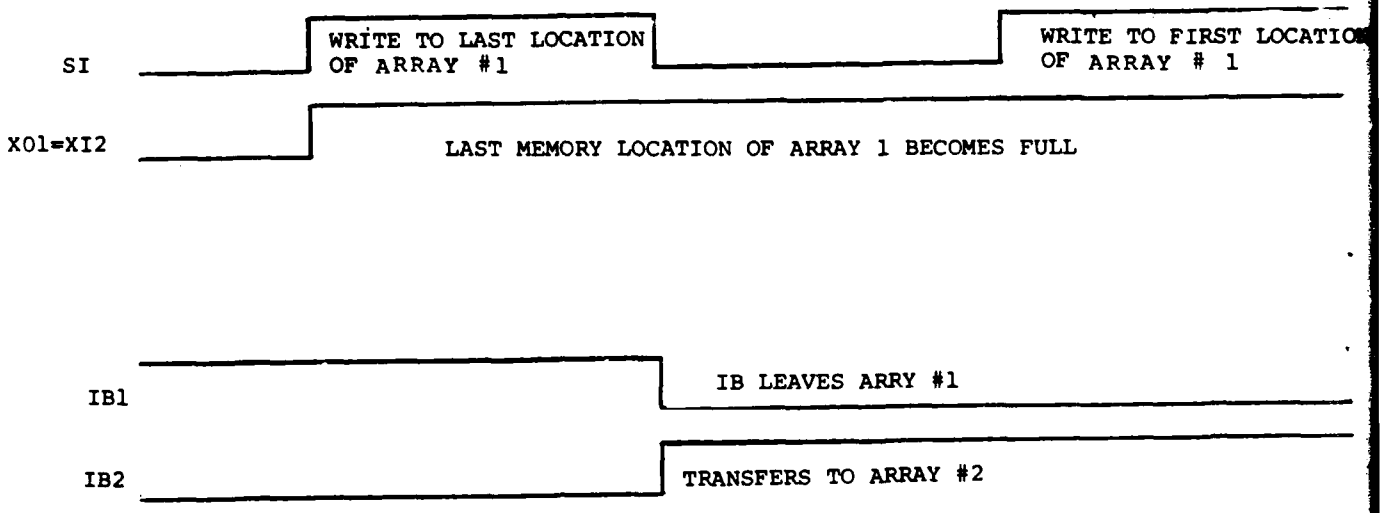
The 5 stage synchronous counter/latch used to count WE and LE pulses is shown in Fig. E-12. Signal CNX is the most significant counter output. CN0, CN1, CN2, and CN3 are the 4 least significant counter outputs. A0, A1, A2, and A3 are the address outputs from the latch following the counter. Although this latch is illustrated as being separate from the counter in Fig. E-4, it is used as part of the counter in Fig.E-12. This saved a number of devices. The counter is asynchronously resettable to zero count and resets when RS=0.

The box labeled FSL in Fig. E-12 is a transmission gate and serves as half of the multiplexer that selects the source of the memory addresses. When FSL is "0", this gate is open and the gate at the output of the retimed input address is transparent so that the address comes from the retimers. When FSL is "1", the counter's transmission gate is transparent while the retimers gate is open so the address comes from the counter. In the following discussion, it is assumed that FSL is "1" and the counters transmission gates are transparent.

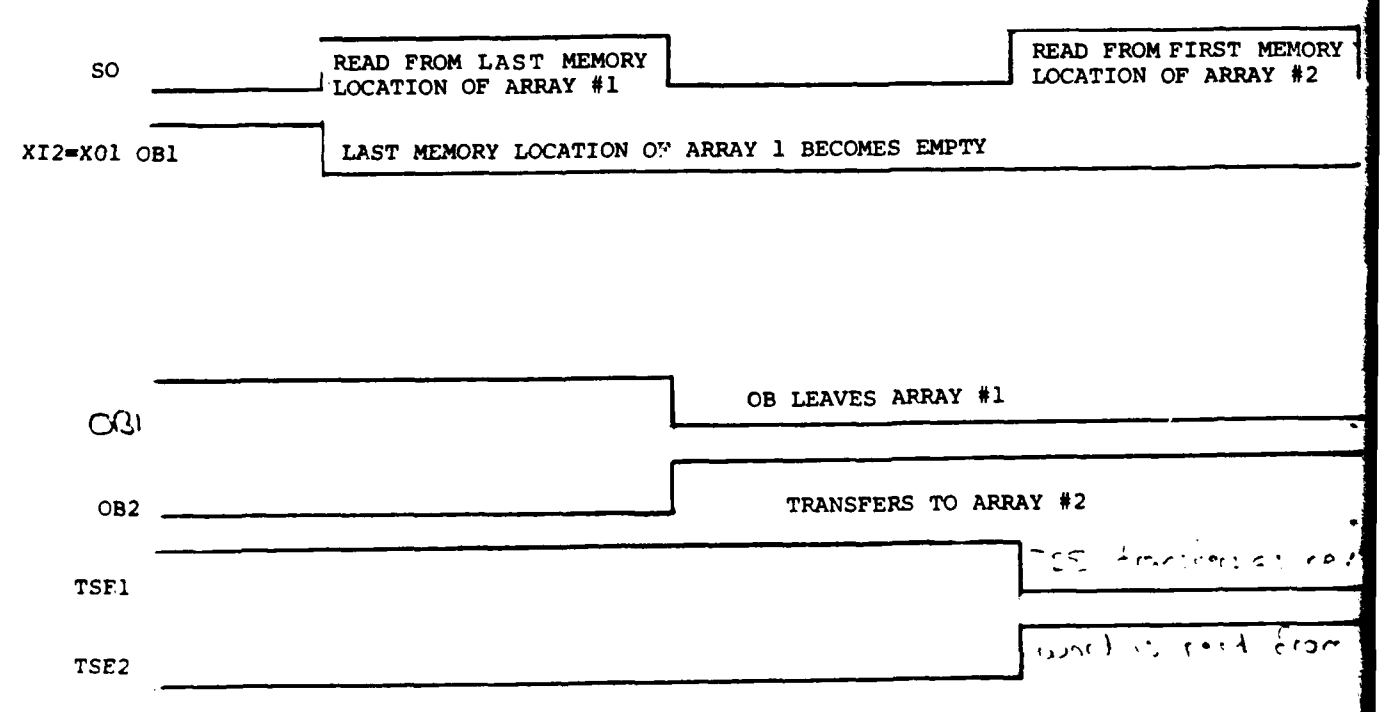
A counter stage toggles on a positive clock edge when all less significant count bits are "1". The first, least significant, stage toggles every time. The next toggles when the first stages count is "1". A following stage toggle when all preceding stages to it have counts of "1"

The T1, least significant, counter stage generates the least significant counter bit. The CN3 signal toggles on every positive transition of clock, C. The A3 signal follows CN3 when C transitions low.

The T2 stage toggles count CN2 only when the CN3 and thereby the A3 signal is a "1" on the positive transition of clock. A2 then follows CN2 on when clock goes low.



CASE I - SHIFTING INTO LAST MEMORY LOCATION



CASE II - SHIFTING INTO LAST MEMORY LOCATION

Figure E-11 BTL Timing Diagrams

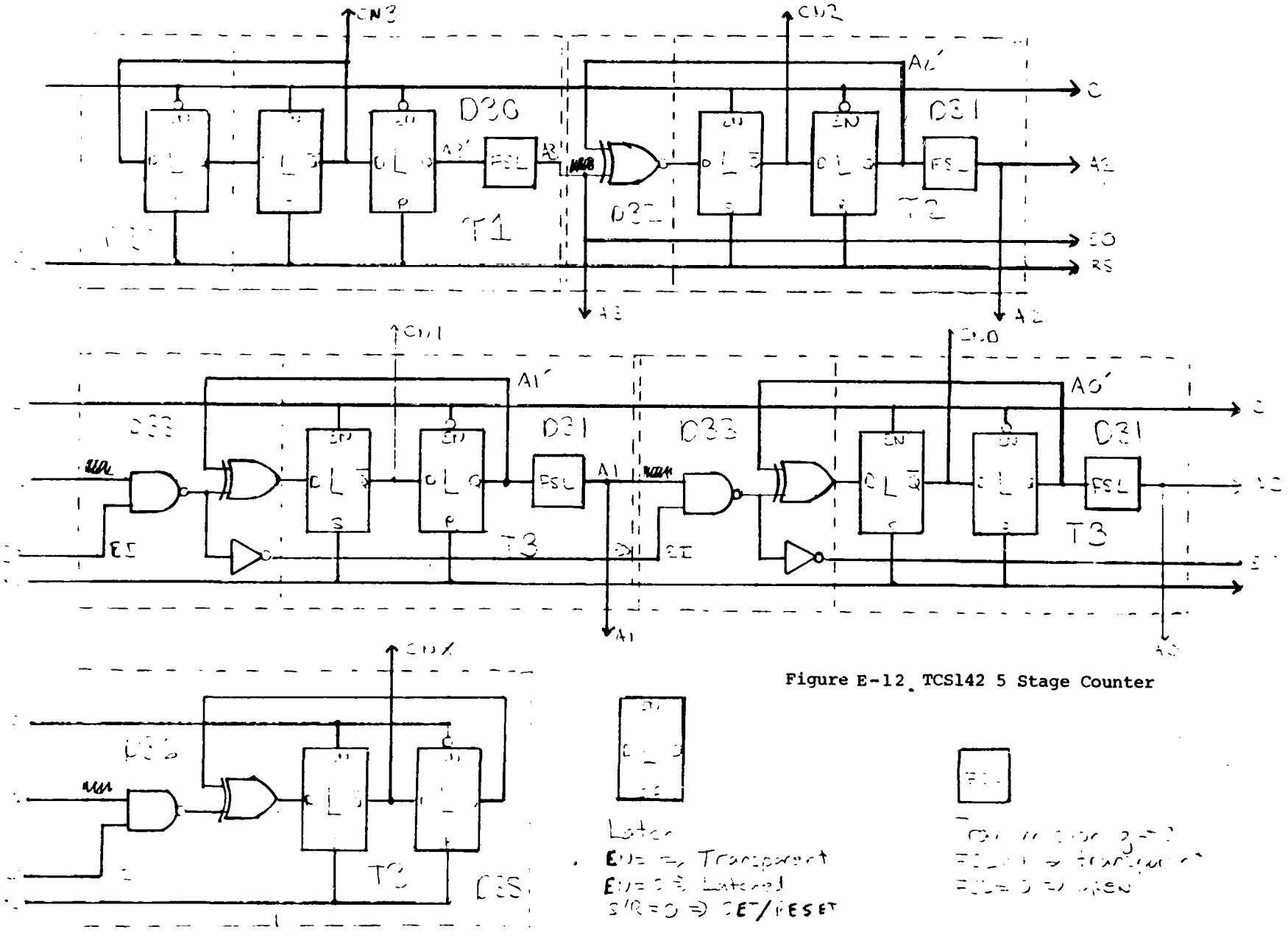


Figure E-12. TCS142 5 Stage Counter

The T3 stages toggle their counts only when the counts of all the preceding stages are "1". This is determined as follows. A stage sends the information that all stages preceding it are "1" through its EO signal. The next stage determines that all stages preceding it are "1" from the combined information of EO signal from the preceding stage and the address bit produced by the preceding stage. The stage then generates its own EO signal from this information which is sent to the next stage. If EO signal is high saying all preceding stages are "1" the count toggles when clock transition is high.

The address bit then follows the count when clock transition is low.

1.2 Memory Design Tradeoff

The multiport memory cell represents the most widely used circuit in the TCS142 and plays a major role in the TCS143 array. Because of its high usage and critical circuit performance, great care was used in the memory circuit schematic selection, design, and simulation. Paramount factors were satisfactory operation over temperature and load variation while maintaining good packing density.

Figure E-13 shows the four memory cell circuit schematics that were considered for the Microsignal Processor program. The type 4 version was not considered in depth because of the significant increase in devices that would be required by its use. Although type 1 has the least number of devices, experience with this configuration has shown problems. A fundamental problem results in the memory cell being upset when either of the READ transmission gates are enabled. The upset occurs when noise on the output has is sufficient to

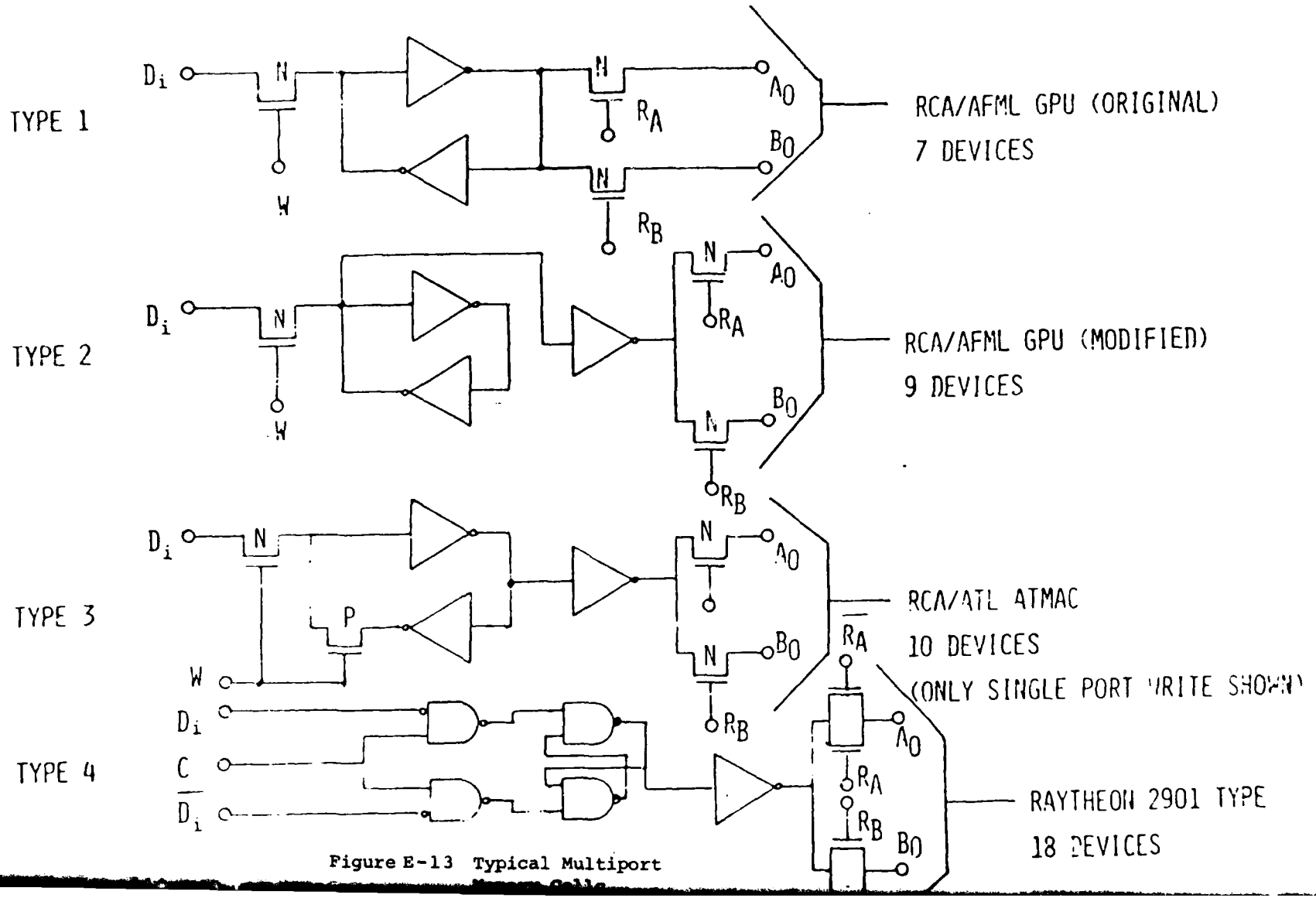


Figure E-13 Typical Multiport Memory Cells

switch the feedback amplifier. Once this occurs, the memory is upset and cannot return to its original state. A modification of this design is shown in type 2 version of Fig. E-13 where an inverter is added to buffer the memory from the READ lines. Version 3 also has the inverter in addition to an additional transmission gate in the feedback loop of the memory. Operating experience has been obtained for both versions 2 and 3 since these have been used in two RCA designed microprocessors. Both of these circuits were selected for detailed analysis and simulations for use on the TCS142.

After simulation of both of these versions, it was seen that version three was less sensitive to transistor parameter variations during a write condition. This is due to the P type transmission gate in the memory feedback path. During a write, the feedback is disabled by this transistor making writing easier. Also, since this additional transistor can be minimum size and its use allows overall device sizing to be less critical, the layout for version three is smaller than that for version two. Both the TCS142 and TCS143 use the type 3 configuration. A schematic of the cell is shown in Fig. E-14 including all device sizes.

The memory has 10 transistors and occupies a 6 mil x 7 mil area resulting in a size factor of 4.2 mil^2/device. Due to this relatively high density, the memory, which constitutes half the transistors of the TCS142, takes only 20% of the area. This memory design is further explored as a simulation example in Section 1.4..

1.3 Multiport/FIFO I/O Signals

The TCS142 array requires 64 I/O Signals to function; namely, 37 input, 26 output, and 1 dual I/O signal. Table E-1 presents the input signals with some descriptive commentary. Table E-2 shows the output signals and

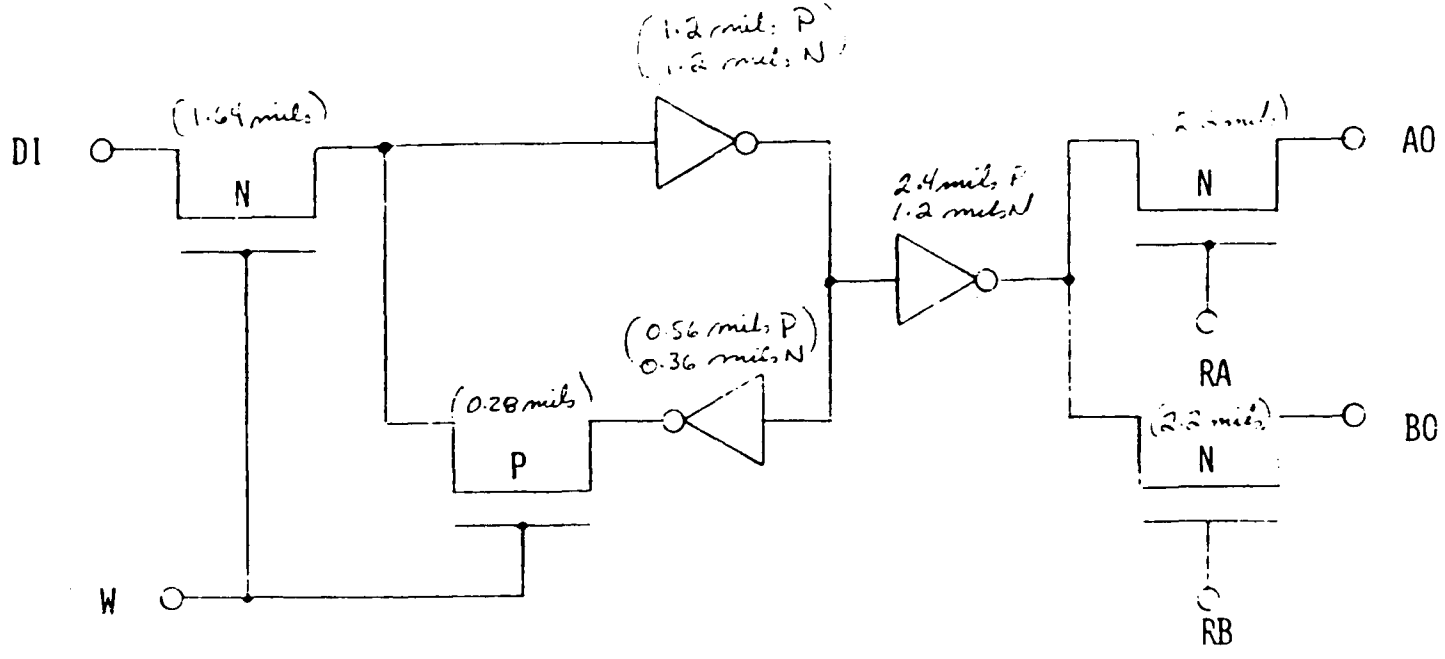


Figure E-14 TCS142 and TCS143 Multiport Memory Cell

TABLE E-1

TCS142 INPUT SIGNALS

Signal Name	Number of Pins
1. Vcc - Power	1
2. Gnd - Return	1
3. DTI (0-11) - Data Inputs	12
4. AAD (0-3) - A Addresses (read)	4*
5. BAD (0-3) - B Addresses (read)	4*
6. WAD (0-3) - Write Addresses When in Multiport mode, all four signals are Write Address inputs. When in FIFO mode, WAD (0), WAD (1), and WAD (2) serve a dual role. WAD (0) becomes FC and serves as a pointer to the First Chip in the FIFO chain. 1 = first chip; 0 = all others. WAD (1) becomes XI, the expansion input. WAD (2) becomes XO, the expansion output and is connected externally to XI of the succeeding chip in the FIFO chain.	4*
7. WINH - Write enable inhibit Logic 1 allows writing to occur with WESI signal. Logic 0 disables writing.	1
8. FSL - FIFO Select When logic 0, the chip is used as a multiport. When logic 1, the FIFO logic is enabled to generate RAM addresses OR and IR.	1
9. LESO - Latch Enable/Shift Out This signal when logic 0 causes the output latches to hold their present value. Logic 1 allows the latches to be transparent. In the FIFO mode, (FSL=1), this signal also is used as a shift out clock.	1
10. RS - Reset Logic 0 forces the latches to logic zero and clears the FIFO logic (IR=1, OR=0).	1*
11. TSEA0 - Tri-state enable for A port latch Logic 1 = enable, 0 = high impedance state.	1*
12. TSEA1 - Tri-state enable for A port latch Logic 0 = enable, 1 = high impedance state.	1*
13. TSEB0 - Tri-state enable for B port latch Logic 1 = enable, 0 = high impedance state.	1*
14. TSEB1 - Tri-state enable for B port latch Logic 0 = enable, 1 = high impedance state.	1*
15. WESI - Write enable/shift in. This signal when high, writes data (DTI) into the memory location specified by the B address. In the FIFO mode it also serves as a shift in the clock.	1
16. MAGC - Logic 0 forces the A port data to a 1 in the MSB followed by all 0's.	1*
17. CLK - Register clock, Rising Edge Trigger.	1
18. SCP - Input bit which is multiplexed to IRSC in the multiport mode. It is anded with sign of data Y_A.	1*
Total Input Pins	38

*T^{2}L Compatible.

TABLE E-2

TCS142 Output Signals

Signal Name	Number of Pins
1. DTA (0-11) - Data out of RAM Port A. Also used as FIFO output.	12*
2. DTB (0-11) - Data out of RAM Port B.	12*
3. IRSC - Input read/sign control. In the FIFO mode (FSL=1). This signal indicates that the FIFO can accept new data. When WESI goes low, IR will also go low. If the FIFO is full, IR will remain low after WESI goes high. Refer to timing waveforms in Section 3.2. In the multiport mode IRSC is a sign control bit whose value corresponds to: SSCP · Sign "Y_A".	1
4. OR - Output Ready. In the FIFO mode (FSL=1). This signal indicates that the FIFO has output data available to be read. When LESO goes high, OR goes low. If the FIFO is empty, OR will remain low after LESO goes high.	1
5. WAD2/XO - FIFO expansion output	**
Total Output Pins	26

*Signals required to drive 50 pf loads with $T_r \leq 25$ ns.

**This lead counted as input.

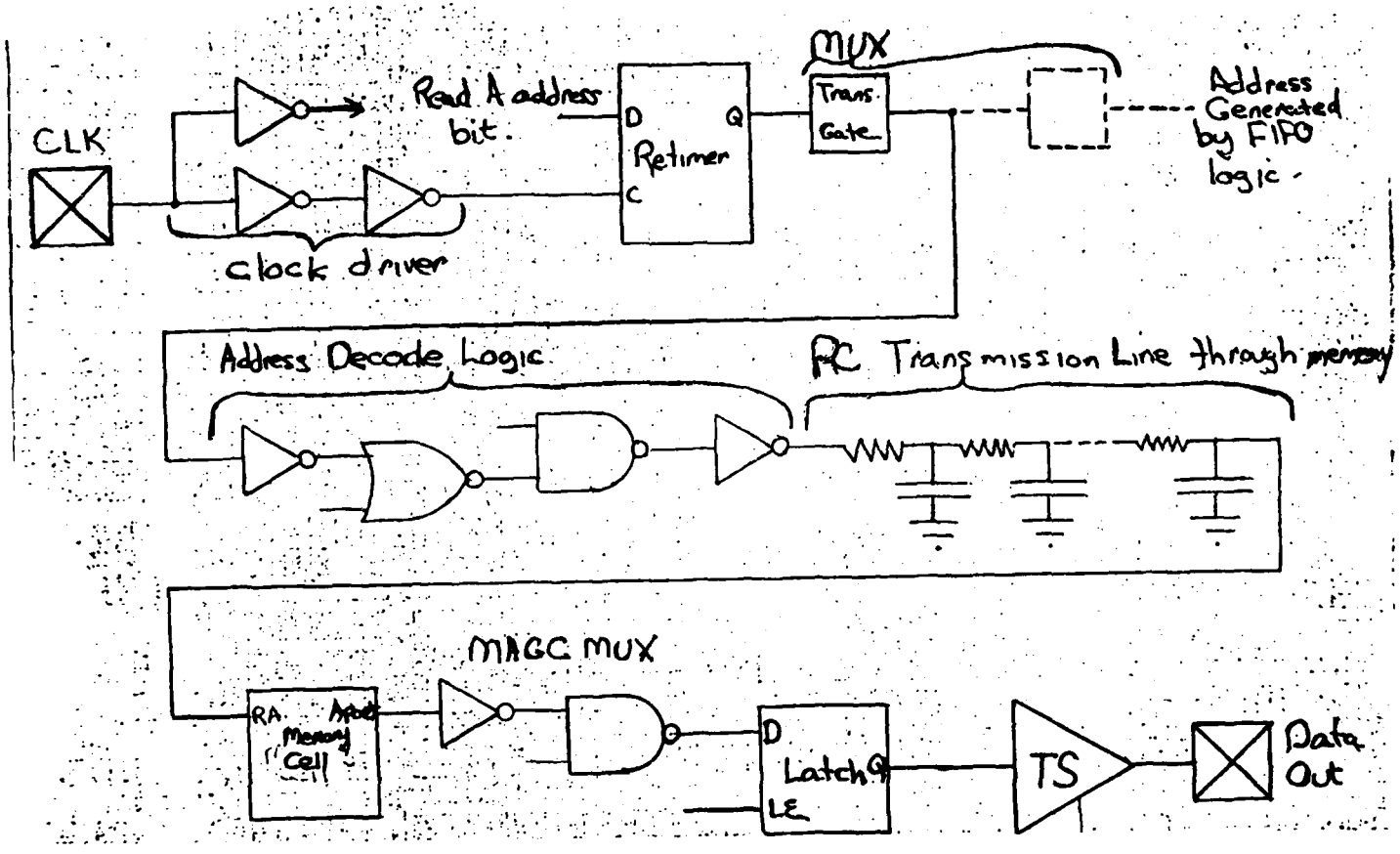


Figure E-15 Access Time Worst-Case Delay Path

identifies those outputs that have been designed to drive 50 pf loads with signal rise times of 25 ns or less.

1.4 Circuit Simulation

Simulations were conducted on each cell in the critical delay path of the TCS142. Also the memory cell, retimer cell and counter cell were carefully simulated to ensure correct operation over a wide range of device parameters. Through these simulations, critical areas in the array design were identified and cells were modified as a result increasing both the speed and design margin of the array. These simulations concluded that the array delays delineated in Section 1.6 could be safely met. As an example of this simulation technique, the array access time calculations are shown in the following paragraphs.

A schematic of the critical access time delay path is shown in Fig. E-15. The critical path is divided into six separate functions for simulation purposes starting with the on-chip delays associated with the clock pulse amplifiers. Using the selected device geometries and parameters, simulations are performed for each of the individual elements. Each circuit load requirement is estimated from the actual design of the subsequent circuit in the chain. The resultant output signal rise and fall times are then used as input signals for the simulation of the following circuit. This method assures signal compatibility and accuracy. Table E-3 shows a summary of the simulation results for the six circuit elements comprising the access time critical path. The results show that 75 ns is the estimated access time. Some design margin has been achieved since specified access time is 90 ns.

An example of a circuit simulation is seen in Figs. E-16 and E-17. This simulation was performed to determine the value of the minimum write pulse width to the multiport array. Figure E-16 shows the circuit that was entered into the RCAP program and simulated. Though the inverters are shown here as logic

symbols, the transistors that make the inverters with their associated device sizes are what is actually entered into RCAP. The simulation output for the minimum allowable write pulse width, 17 ns, is shown in Fig. E-17. The waveforms are identified by name and number for cross reference with the schematic of Fig. E-16. The idealized waveform $\overline{WE}$, (1), is shown as the input to the Write Enable decode structure. The WE, (2), signal appearing at the input to the memory cell is degraded due to the action of the transmission line effect of the line passing through the memory. For this example, a data "1" is being written into the memory location. As seen in Fig. E-17, the memory output line, (3), is driven from a "0" to a "1" with a slight perturbation occurring at about 5 volts--the switching point for the memory cell.

This perturbation indicates the beginning of an unstable condition and that any reduction in the WE signal may cause the memory not to store the new input bit. In fact, a second simulation using an input $\overline{WE}$ width of 16 ns failed to store the "1", thereby setting the minimum pulse width at 17 ns.

1.5 Multiport/FIFO Cell Description

The TCS142 array is comprised of 39 active circuit cell types and 20 inactive cells for a total of 59 total cells. The active cells contain all the circuits associated with the Multiport/FIFO logic implementation. The inactive cells contain interconnecting wiring, array nomenclature alphanumerics, alignment keys and test transistors.

Table E-4 lists the various cell types and names of all cells along with the number of devices in each cell, the number of times used, and total device count for the array. The table lists common cells that were designed for the TCS140 and selected for use on the TCS142.

Figure E-18 is a map of the TCS142 showing the location of the various cells. This map can also be compared to the composite array checkplot of Figure E-20. The cell definitions (D numbers) shown in Fig. E-18 have the prefix "D" missing but otherwise are identical to those listed in Table E-4.

1.6 Design Specifications

The electrical design specifications for the TCS142 performance are given in Tables E-5 through E-8. An interface timing diagram for FIFO operation is shown in Fig. E-19.

Like the TCS140, the TCS142 has been designed to operate over the temperature range of -55°C to +125°C within the specifications given in the tables. The significant increase in quiescent current over the TCS140, however, is due to the T^2L compatible input requirement. Although CMOS circuitry does not normally have a DC current requirement, the level shift circuits to operate with T^2L (with only an array power supply of 10 Volts) requires DC current. Thirty T^2L level shifters will require approximately 4 mA worst case to establish the proper T^2L to CMOS switching voltage.

Tables E-7 provides the 25°C Multiport related delay time for various signal paths. These delays have been specified by Raytheon system designers and have served as the design baseline for the RCA design effort. The FIFO 25°C performance requirements are delineated in Table E-8. All delays are for 10 Volt operation.

TABLE E-3

ACCESS TIME SIMULATION SUMMARY

Cell Simulated	Delay
Clock Driver	10 ns
Retimer and MUX	8 ns
Address Decode and RC Transmission Line	21 ns
Memory Cell and MAGC MUX	12 ns
Latch	8 ns
Tristate	16 ns
Access Time	75 ns

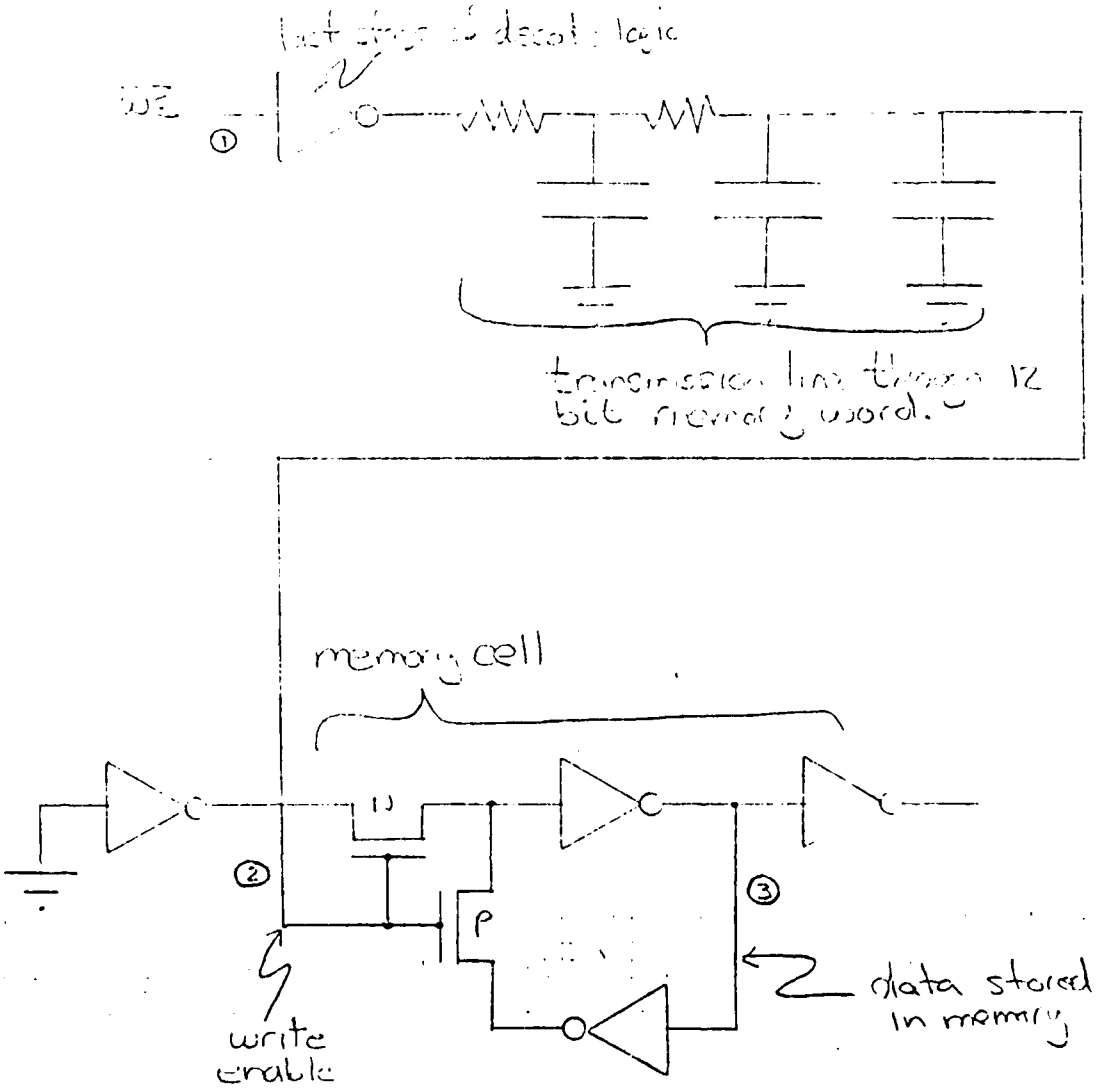


Figure E-16 Circuit to Determine Minimum Write Pulse Width

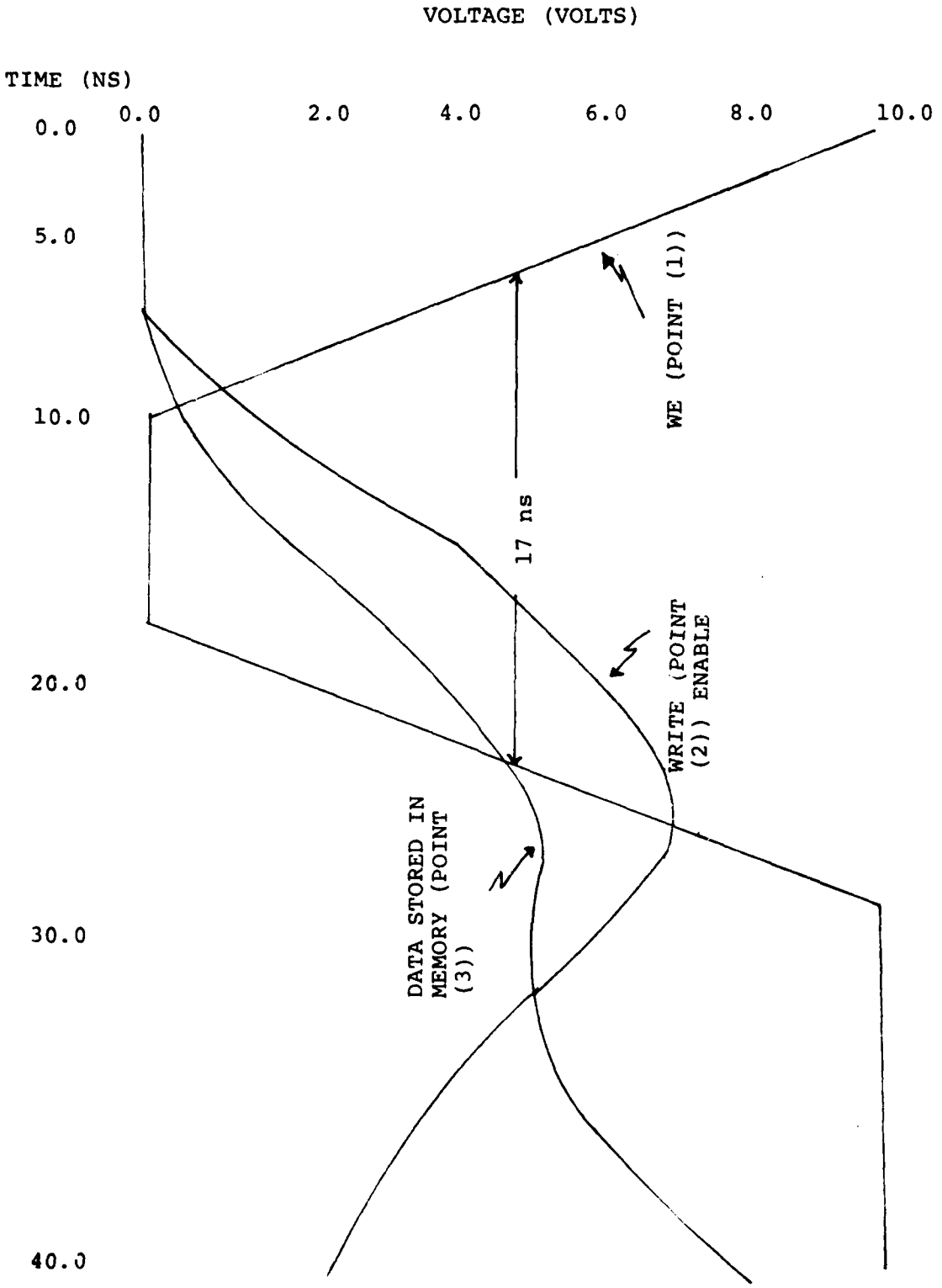


Figure E-17 RCAP Simulation of Minimum Write Pulse Width

TABLE E-4

CUSTOM CELLS FOR TCS142

Cell #	Cell Name	# Of Times Used	# Of Devices	Total Devices
D1	Memory Cell	192	10	1920
D2	Memory Buffer MAGC MUX	11	10	110
D3	Memory Buffer MAGC MUX	1	10	10
D4	Memory Input Inv.	12	2	24
D10	A+W Decode	16	14	224
D11	B Decode	16	6	96
D12	Decode	4	6	24
D13	Decode	8	6	48
D14	Decode	4	6	24
D15	Decode	2	6	12
D16	Decode	4	6	24
D17	Decode	2	6	12
D20	Latch	24	7	168
D30	Resettable Retimer with MUX	2	19	38
D31	Resettable Retimer with MUX	6	19	114
D32	XNOR	2	4	8
D33	CE Logic	4	8	32
D34	Counter Interconnect #1	6	-	-
D35	Resettable Retimer	2	17	34
D36	CE Logic	2	8	16
D37	Settable Latch	2	9	18
D38	Counter Interconnect #2	2	-	-
D60	Retimer with MUX	2	18	32
D61	Retimer with MUX	6	18	108
D63*	Retimer	9	16	144
D64	Retimer	1	16	16
D70	Tristate	1	8	8
D71	Tristate	1	8	8
D73	Tristate	10	8	80
D74	Tristate	12	8	96
D75	Tristate	2	8	16
D76	Tristate	1	8	8
D81*	Input Inverter + Pad	4	2	8
D82*	T^2L to CMOS + Pad	8	8	64
D83	T^2L to CMOS + Pad	22	8	176
D90	TS Control + Inverter	1	36	36
D91	Comparator	1	52	52
D92	BT Logic	1	76	76
D93	OR + IRSP Logic	1	24	24
D94	LE + SS	1	12	12
D95	Cell Interconnect	1	-	-
D96	WE, CLK, FSL Logic	1	16	16
D100	TCS142	1	-	-
D101*	Level Numbers	1	-	-
D103*	PLY	1	-	-
D104*	N+	1	-	-
D105*	CNT	1	-	-
D106*	MET	1	-	-
D107*	PAD	1	-	-
D108*	LD	1	-	

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UNCLASSIFIED BR-13111 AFWAL-TR-82-1071 NL

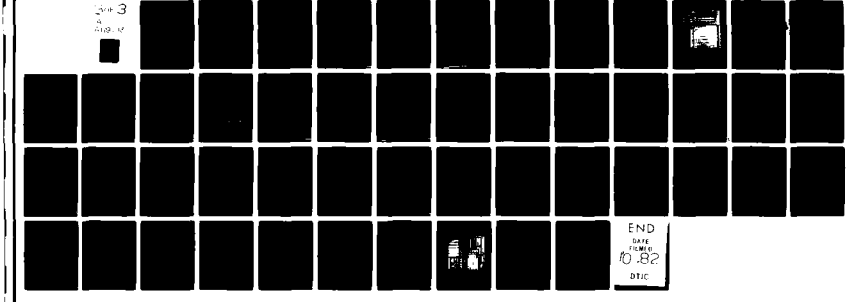


TABLE E-4
CUSTOM CELLS FOR TCS142 (Cont.)

Cell #	Cell Name	# Of Times Used	# Of Devices	Total Devices
D109*	P+	1	-	-
D111*	Alignment Dark Field	1	-	-
D112*	Alignment Light Field	1	-	-
D113*	Test Transistor	1	-	-
D140	Array Interconnect	1	-	-
D141	Array Interconnect	1	-	-
D142	Array Interconnect	1	-	-
D143	Array Interconnect	1	-	-
D144	Array Interconnect	1	-	-
			Total Devices	3936

*Cells common to TCS140.

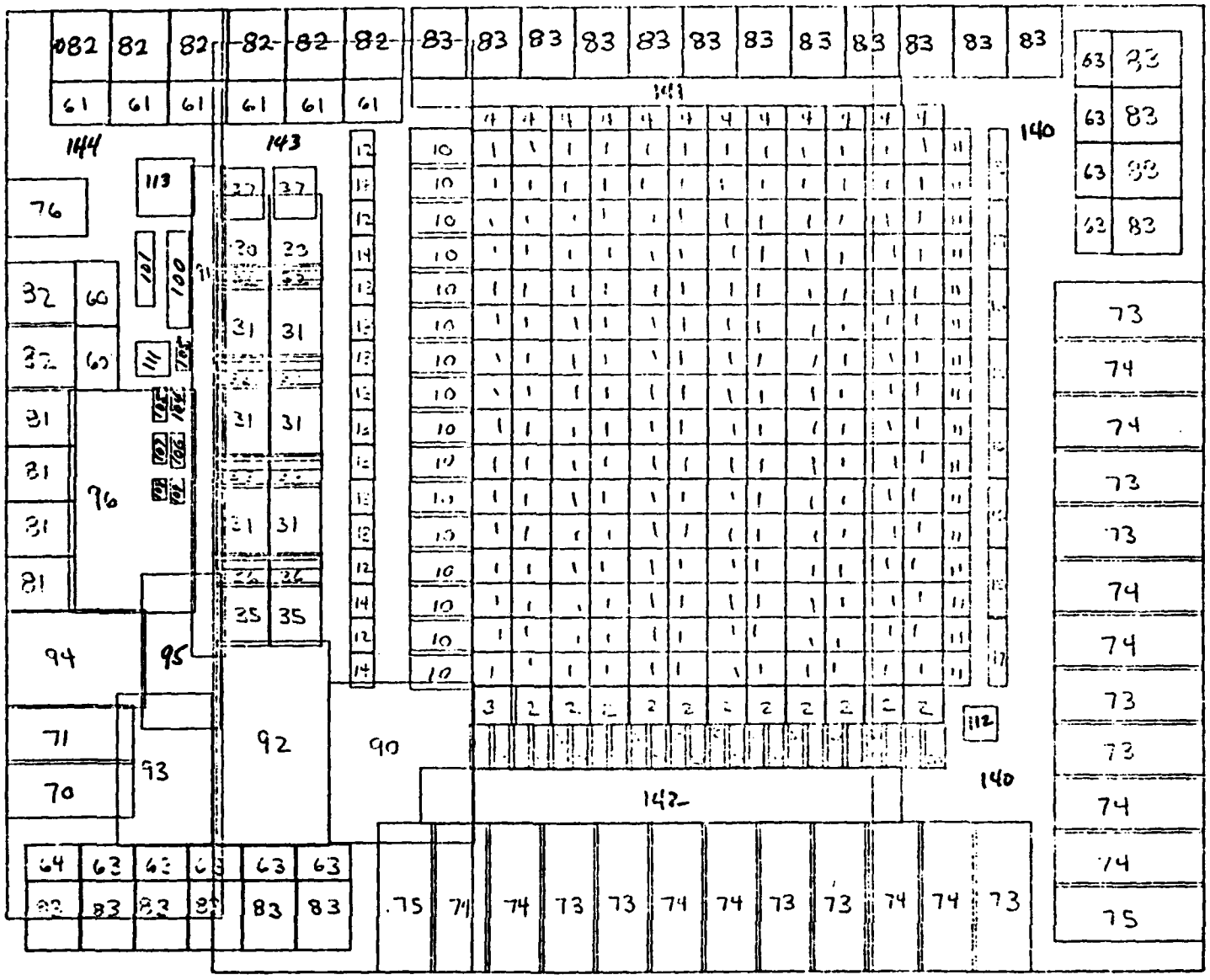


Figure E-18 Cell Map of TCS I42

NOTE NUMBERS ARE DXX CELL DESIGNATIONS.

TABLE E-5
STATIC SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	$-55^{\circ}C$ to $+125^{\circ}C$
Non-operating	$-65^{\circ}C$ to $+150^{\circ}C$
Supply Voltage	+15V non-operating
Input Voltage	-.5V to (Vcc + .5V)

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	3	4	mAmp
VOL Ouput Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input [1] Low	5 10	-	-	1.5 3.0	Volts
VIH Input [1] High	5 10	3.5 7.0	-	-	Volts
IO Outputs Sink and Source	5 10	-	1.5 1.5	within .5V of Supply or GND	MA
Iin Input [2] Current	0< Ein < Vcc	-	.3	1	µamp
Cin data/ clock	any	-	2	3/5	pf
Vcc	-	4.5	10	12	Volts

NOTES: 1. Input voltage for T^2L compatible inputs: VIL=0.8 V max, VIH=2.0 V min.

2. Iin for T^2L = 200µA

TABLE E-6

SWITCHING CHARACTERISTICS

CHARACTERISTICS	Vcc	Min	Typ	Max	Units
Output Rise and Fall Time (15pf Load)	5 10	-	30 15	40 18	nsec nsec
Data Setup Time [1]	10	-	5	7	nsec
Data Hold Time	10	-	8	10	nsec
Clock Width	any	50	75	-	nsec
Clock Rate	5 10	- 6.66	3 6.66	- -	MHz MHz
Clock to Output (LE $\Rightarrow$ 1)	10	-	15	20	nsec
PD @6.6 MHZ	10	-	300	-	mW

1. Applies to input control registers

TABLE E-7

MULTIPORT SWITCHING PARAMETERS

	MIN	TYP	MAX
Access Time	-	35	90 nsec
Write Pulse Width	50	75	N/A nsec
RESET Pulse Width	50	75	N/A nsec
RESET Delay	-	25	50 nsec
ENABLE Time (LE→1)	-	15	30 nsec
Input Address Setup Time[1]	-	-	5 nsec
Input Data/Address Hold Time[2]	-	-	5 nsec
Input Data Setup Time[3]	-	-	40 nsec

1. Prior to Rising Edge of WE
2. After Falling Edge of WE
3. Prior to Falling Edge of WE

TABLE E-8

FIFO SWITCHING SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	
Shift In Rate	6.6	6.66	-	MHz
Shift Out Rate	6.6	6.66	-	MHz
WESI Width (low)	50	75	-	nsec
LESO Width (high)	50	75	-	nsec
Input Ready on Delay (TIRL)*	10	15	20	nsec
Input Ready Off Delay (TIRH)*	10	15	30	nsec
Output Ready Off Delay (TORL)*	10	15	30	nsec
Output Ready On Delay (TORH)*	10	15	30	nsec

*See Waveforms - Figure E-19 .

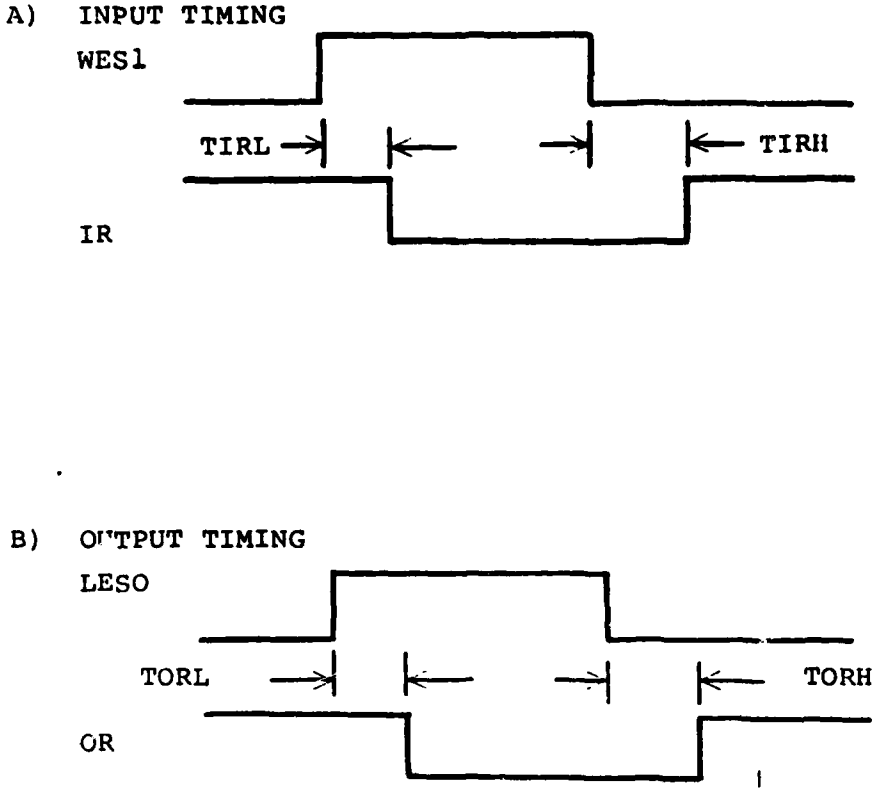


Figure E-19 IR/OR Timing Diagram

1.7 Test Word Generation

The TCS142 logic diagram was approved after the logic was verified using the TESTGEN logic simulator. A test pattern was then generated that will test the TCS142 in both the FIFO and Multiport modes of operation.

The method of generating the computer model was similar to that used in the TCS140 with one exception. In the TCS140, the array logic was generated from an interconnection list of macros. These macros were generated by the designer. In the TCS142, however, the macros used to generate the array logic were generated from simpler macros and these in turn from still simpler macros. By breaking the array logic into several large macros it was easy to check the logical validity of each macro saving considerable effort in checking the array logic model.

One test that was done in this manner was to connect two FIFO control logic macros together as they would be when the FIFO's operate in the expanded mode. This allowed testing the expandability of the FIFO without connecting two entire array logic models together.

When the TCS142 logic was verified, a test pattern was generated. The test pattern is divided into two sections 1) FIFO operation and 2) multiport operation. The first 71 test patterns were used to test the array in the FIFO mode. Tests involved shifting 16 data words into the FIFO and subsequently shifting them out. This tests all the FIFO address generating logic, expansion logic, and full and empty state detection logic. The next 962 tests test the array in the multiport mode. In these tests, data is read into and read out from each memory location to verify those locations. The test patterns are the ones

suggested by Raytheon. Seven basic memory patterns are tested at each memory address on both output ports. They are as follows:

1. All ones
2. All zeros
3. Walking ones
4. Walking zeros
5. Alternating 1's and 0's (hex AAA)
6. Alternating 0's and 1's (hex 555
7. Data = Address

In summary, the test sequence for the TCS142 is 1043 words by 63 bits and tests 95% of all circuit faults.

1.8 Physical Characteristics

Figure E-20 is a composite checkplot of the final input configuration of the TCS142. The large block of repetitive polygons is the 16 word by 12 bit memory that serves as the basic storage for the Multiport and FIFO functions.

All seven layers required by the CMOS/SOS process are shown.

The array size is 177 mils by 221 mils and contains 3936 transistors. Using these dimensions, the array device size factor is 9.9 mil^2 per device. This factor is larger (less dense) than that for the multiplier and reflects the impact of the random type logic associated with the FIFO control logic.

The 64 active leads require that the TCS142 be packaged in either a 64 lead DIC or 64 pin LHP as described for the TCS140. A bonding diagram is shown in Fig. E-21 and a listing of the pinouts is shown in Table E-9.

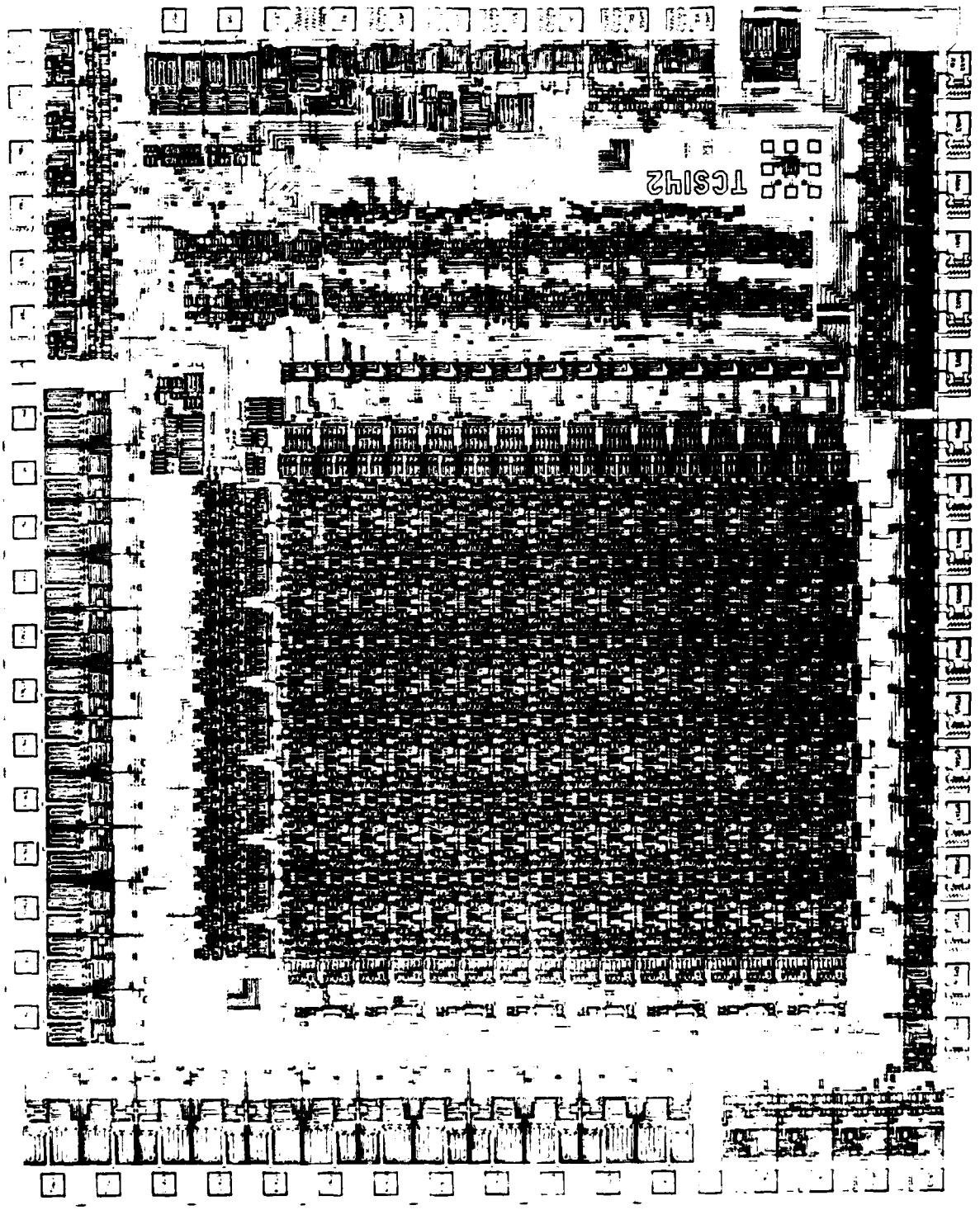


Figure E-20 TCS142 Composite Checkplot

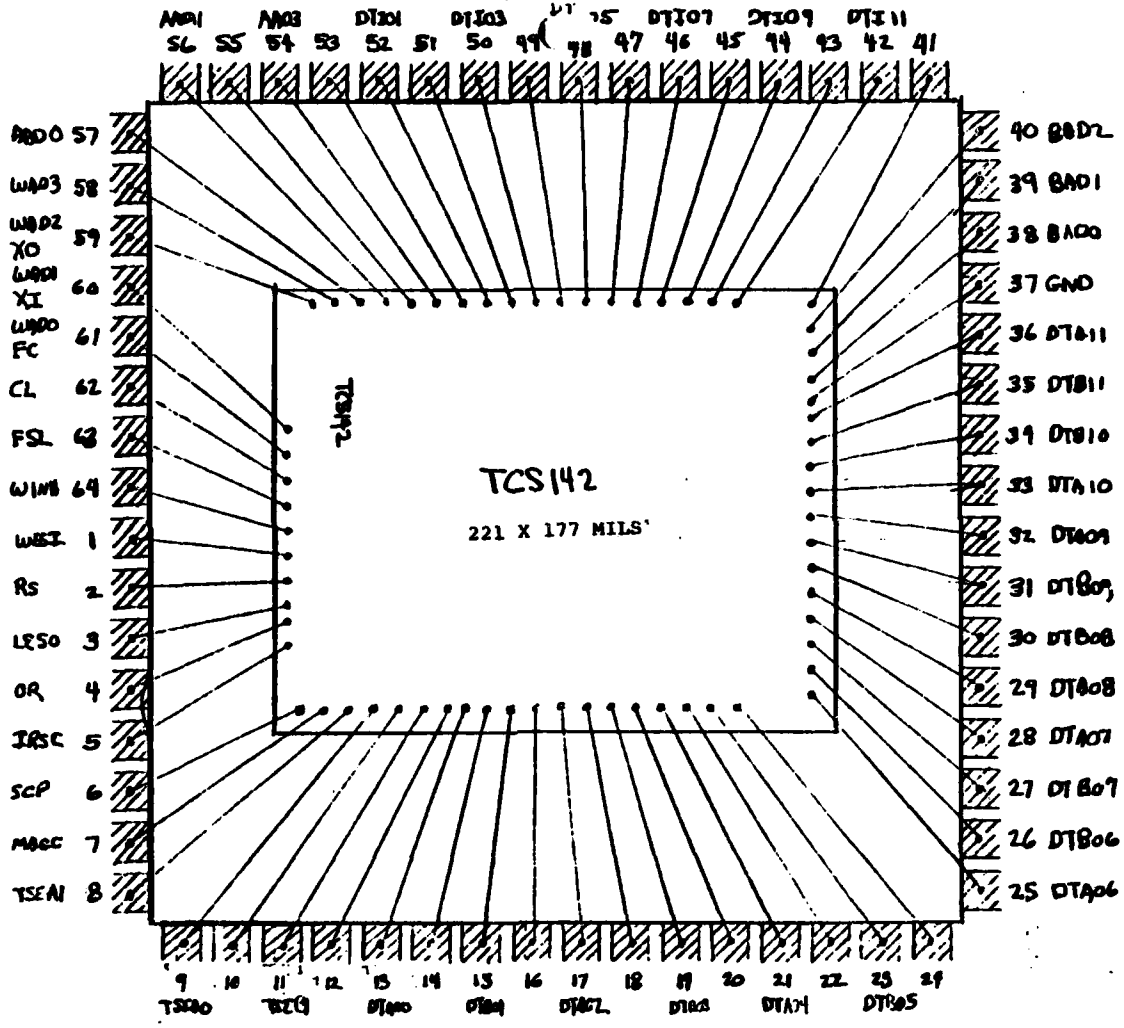


Figure E-21 TCS142 Bonding Diagram

TABLE E-9

PINOUT LISTING

Pin #	Signal Name	I/O	Pin #	Signal Name	I/O
1	WESI	I	33	DTA10	0
2	RS	I	34	DTB10	0
3	LESO	I	35	DTB11	0
4	OR	0	36	DTA11	0
5	IRSC	0	37	GND	I
6	SCP	I	38	BAD0	I
7	MAGC	I	39	BAD1	I
8	TSEA1	I	40	BAD2	I
9	TSEA0	I	41	BAD3	I
10	TSEB0	I	42	DTI11	I
11	TSEB1	I	43	DTI10	I
12	VDD	I	44	DTI09	I
13	DTA00	0	45	DTI08	I
14	DTB00	0	46	DTI07	I
15	DTB01	0	47	DTI06	I
16	DTA01	0	48	DTI05	I
17	DTA02	0	49	DTI04	I
18	DTB02	0	50	DTI03	I
19	DTB03	0	51	DTI02	I
20	DTA03	0	52	DTI01	I
21	DTA04	0	53	DTI00	I
22	DTB04	0	54	AAD3	I
23	DTB05	0	55	AAD2	I
24	DTA05	0	56	AAD1	I
25	DTA06	0	57	AAD0	I
26	DTB06	0	58	WAD3	I
27	DTB07	0	59	WAD2/XO	I/O
28	DTA07	0	60	WAD1/XI	I
29	DTA08	0	61	WAD0/FC	I
30	DTB08	0	62	CL	I
31	DTB09	0	63	FSC	I
32	DTA09	0	64	WINH	I

APPENDIX F
TCS143 DESCRIPTION

1.0 DETAILED DESCRIPTION OF TCS143

1.1 Functional Description of Scaler/Shifter TCS143

The scaler/barrel shifter LSI array, also known as the TCS143, performs several scaling and data manipulations under micro code control. The array can shift (scale) 12 bits of input data based on either exponent (floating point), leading zero count (fixed), an external shift factor, or combinations of these factors. A block diagram of the TCS143 array is shown in **Fig. F-1.**

The functions of the TCS143 can be subdivided into five logical blocks as follows:

1. Order memory to hold and reorder incoming data, while the appropriate shifts are being calculated.

2. Lead zero count logic to compute the number of leading zeros in the incoming data.

3. Scale register logic which operates on either the leading zero count or exponent, or both, to determine the largest number in a given set of numbers. Based on these operations, scale factors are generated to be used by the shift count generator.

4. Shift count generator which produces the shift count using the scale factors produced by the scale register logic and scale factors externally supplied.

5. The shift barrel which scales the data and/or strips the exponents from the magnitude.

Each of these functional blocks is described in more detail below.

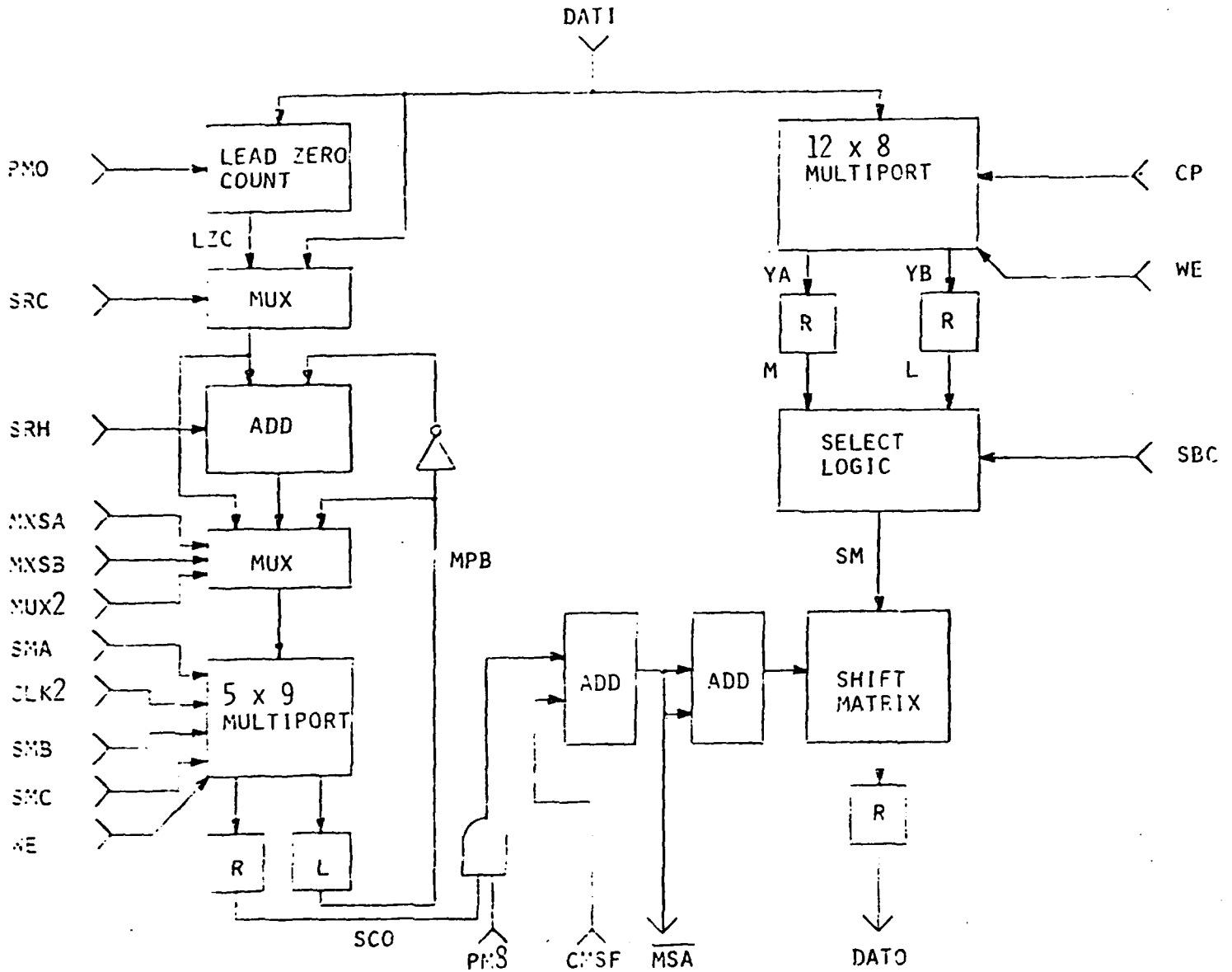


Figure F-1 Pipeline Scale Chip Block Diagram

1.2 Lead Zero Count

The lead zero count logic shown in Fig. F-2 determine the number of leading zeros in the incoming data (leading ones in the case of negative numbers). The control bit (PMO) allows the input to be signed (PMO=1) or a magnitude only (PMO=0). The design of the lead zero count logic uses three four-bit priority encoders which count leading ones. Hence, each bit in a positive or unsigned number is inverted prior to input to the priority encoders. A negative number is supplied to the priority encoders without any inversion. The final output of the lead zero count is a four bit number with a minimum value of zero for no leading zeros and a maximum value of 12 for all zeros. If the output of the priority encoder operating on the four leading bits is less than four, the output of this priority encoder is the desired lead zero count. If the output of the priority encoder operating on the four leading bits is four, the priority encoder operating on the middle four bits is examined and, if its output is less than four, the lead zero count equals the output of the middle priority encoder plus four. In cases where the outputs of the first two priority encoders are four, the lead zero count is the output of the priority encoder operating on the least significant bits with a factor of eight added in.

1.3 Scale Register Logic

The scale register logic contains an adder which performs a subtract function. This subtract operation, in conjunction with memory and a multiplexer, allows selection of data based on the smaller of two numbers. In processing the data in the pipeline, this function allows scaling to the largest number in a set of numbers.

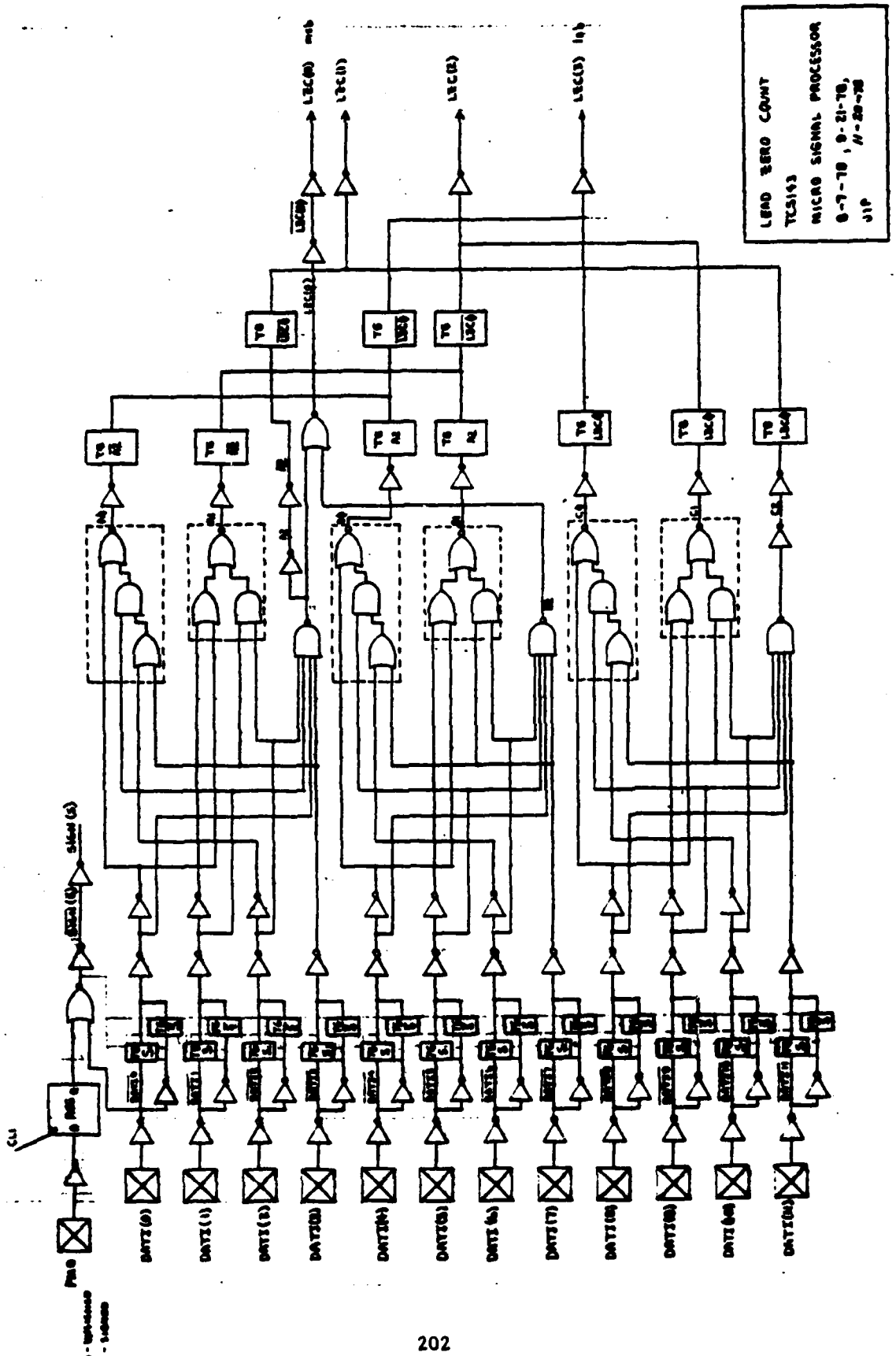


Figure F-2 Lead Zero Count

The SRC input controls the multiplexer selecting one of the inputs to the scale register logic adder (Fig. F-3). When SRC is high and five LSBs of the input data are selected (floating point exponent). The leading zero count is selected as the adder input when SRC is low. The sign bit of the selected input is controlled by the SRH input allowing the exponent to be signed (2's complement) or unsigned magnitude. The sign bit is formed by ANDing the SRH input with the DATI(7). The second input to the adder is the 2's complement of the B port output from the scale register logic multiport memory. Hence, the adder subtracts the selected stored exponent from the incoming exponent or lead zero count.

The remaining scale register logic in Fig. F-3 selects the input to the multiport based on the MXSA, MXSB, and MUX2 inputs as shown in Table F-1. When both MUX2 and MXSB are low the new data is selected for entry into the multiport memory. When MUX2 and MXSA are low and MXSB is high, the memory feedback data is selected for entry into the multiport memory. When MUX2 is low and both MXSA and MXSB are high, the sign bit from the subtractor is used to control the selection of the smaller number between the feedback data and the new data. Finally, when MUX2 and MXSB are both high and either MXSA or the sign bit is low, the output of the adder is the selected multiport input. The remaining unused combinations result in the logical OR of the input data with the adder output as the multiport input. Consequently, this logic permits either the old data, the new data, the smaller of the two, or their difference (new minus old) to be written into the multiport memory.

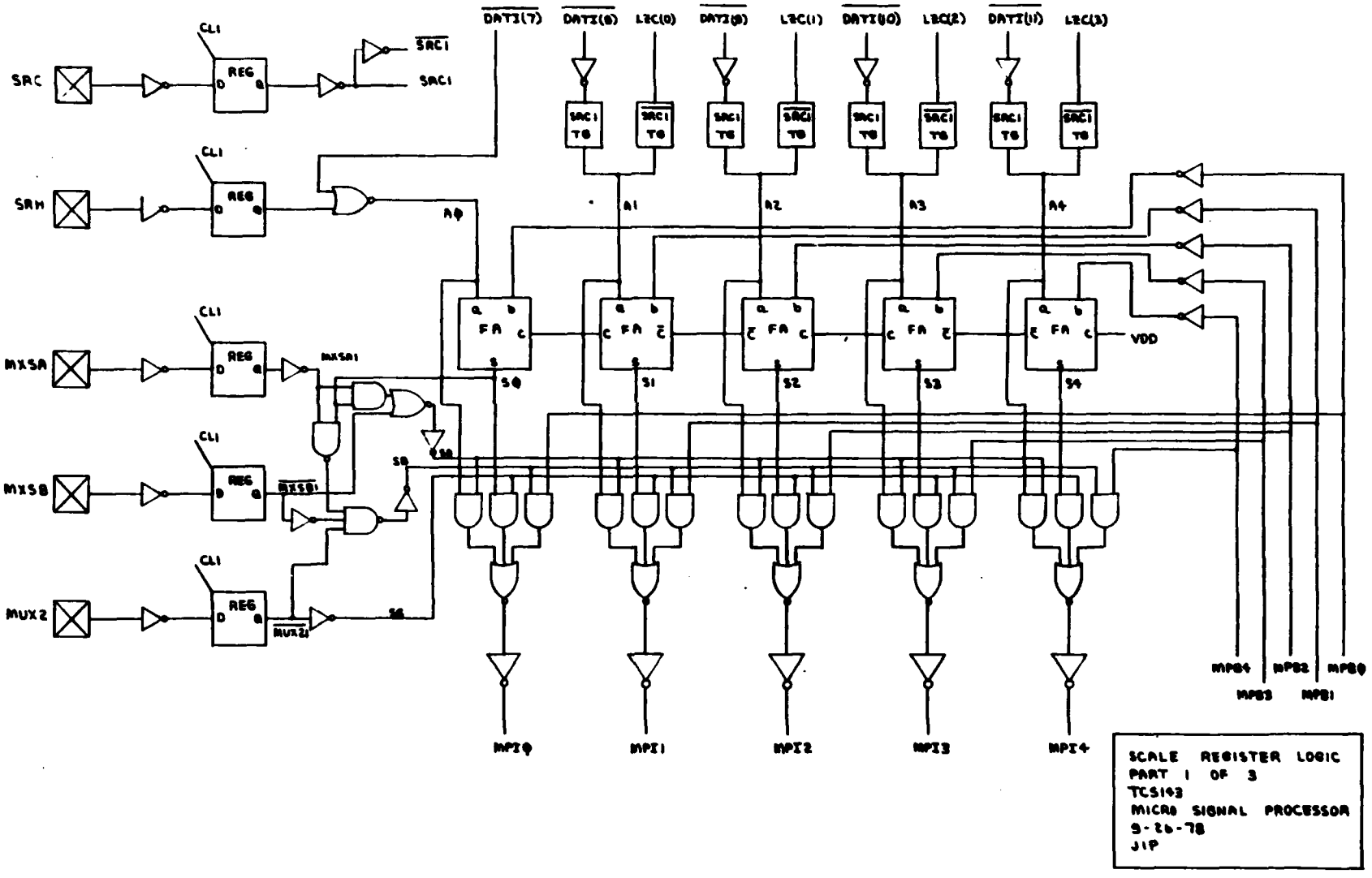


Figure F-3 Scale Register Logic (Part 1)

TABLE F-1

SCALE REGISTER MULTIPORT INPUT SELECT

MUX2	MXSB	MXSA	SIGN	MPI
0	0	0	0	A
0	0	0	1	A
0	0	1	0	A
0	0	1	1	A
0	1	0	0	B
0	1	0	1	B
0	1	1	0	B
0	1	1	1	A
1	0	0	0	S + A
1	0	0	1	S + A
1	0	1	0	S + A
1	0	1	1	S + A
1	1	0	0	S
1	1	0	1	S
1	1	1	0	S
1	1	1	1	S + A

A - OUTPUT OF LZC OR DATI SELECT
B - OUTPUT FROM MULTIPORT B PORT
S - OUTPUT OF A-B SUBTRACTOR
S+A - LOGIC OR

The Scale Register Logic's multiport contains nine words of five bits each as shown in Fig. F-4. The nine addressable locations are coded 0000 and 1000 through 1111. The memory cells are identical to those used on the TCS142 Multiport/FIFO array with a single write port and two read ports. The address for writing is defined by the SMC array inputs with actual entry occurring when the write pulse WE is low. The A port address is defined by the CLK2 and SMA array inputs with only memory locations 1000 through 1111 accessible on this port. The B read port address is defined by the SMB inputs with all memory locations accessible on this port.

The outputs on both the A and B ports are entered into latches controlled by the array clock CL1. When CL1 is high, the latches are transparent, but when CL1 is low, the memory output present when CL1 goes low is held in the latch. Thus, the output of the latch is not changed if new data is written into the addressed location by WE while CL1 is low. This allows the same memory location to provide the old data to the scale register logic and to receive the new data entry via the write port. The output on the B port is fed back to the scale register multiport input logic. The output on the A port passes through a second latch controlled by the opposite phase of CL1 and constitutes the SCO input to the shift count generator. The two latches in series on the A port form a master/slave register with transitions occurring on the negative going edge of clock CL1.

Each of the control inputs to the scale register logic is retimed on chip using the CL1 clock as shown in Fig. F-5. The four bits in the write address SMC and the B port read address SMB are also retimed on chip as shown in Figure F-5. The two least significant bits of the A port address pass through a four stage shift register while the third bit of the A port address is not retimed as shown in Fig. F-5.

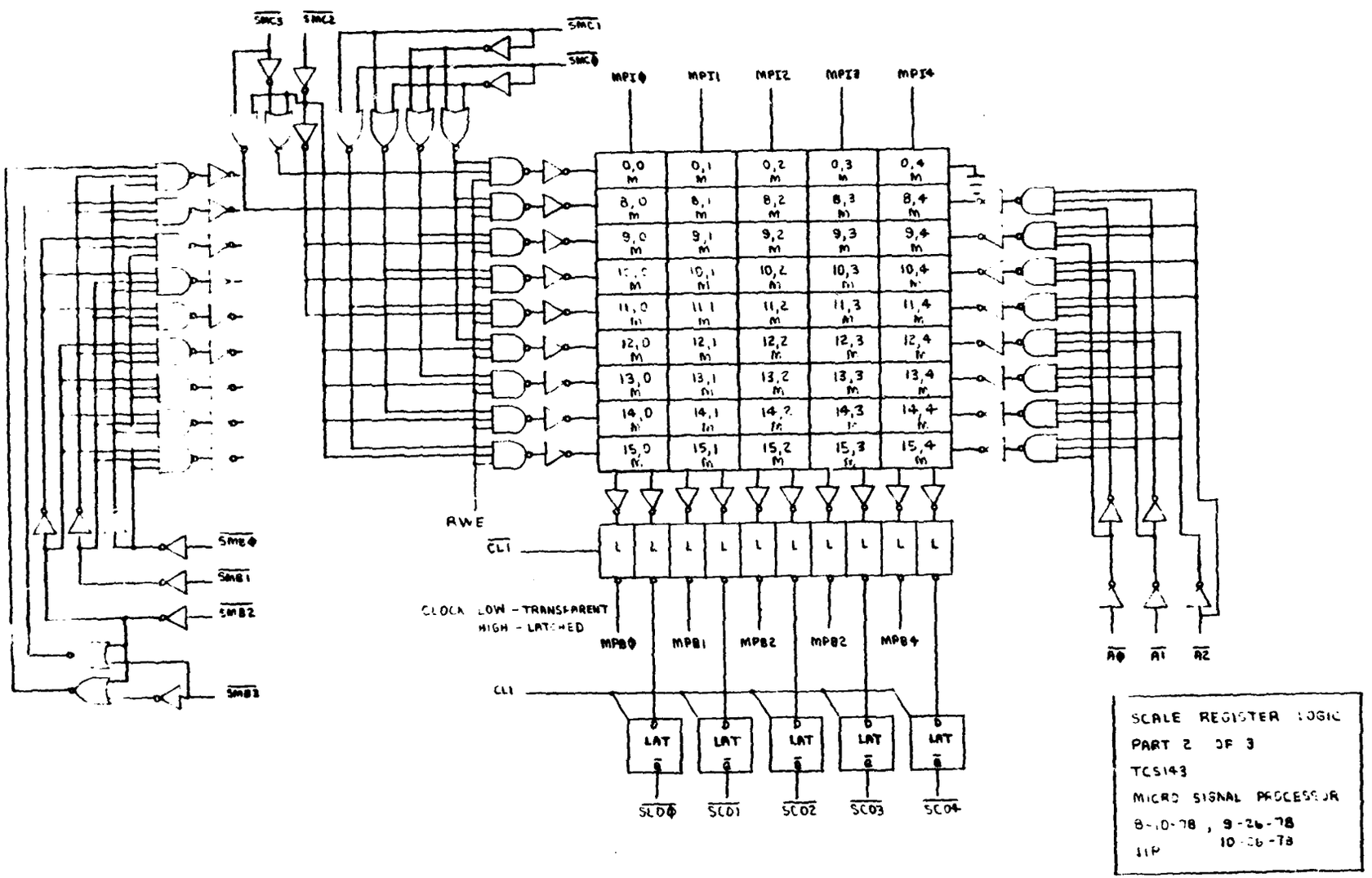
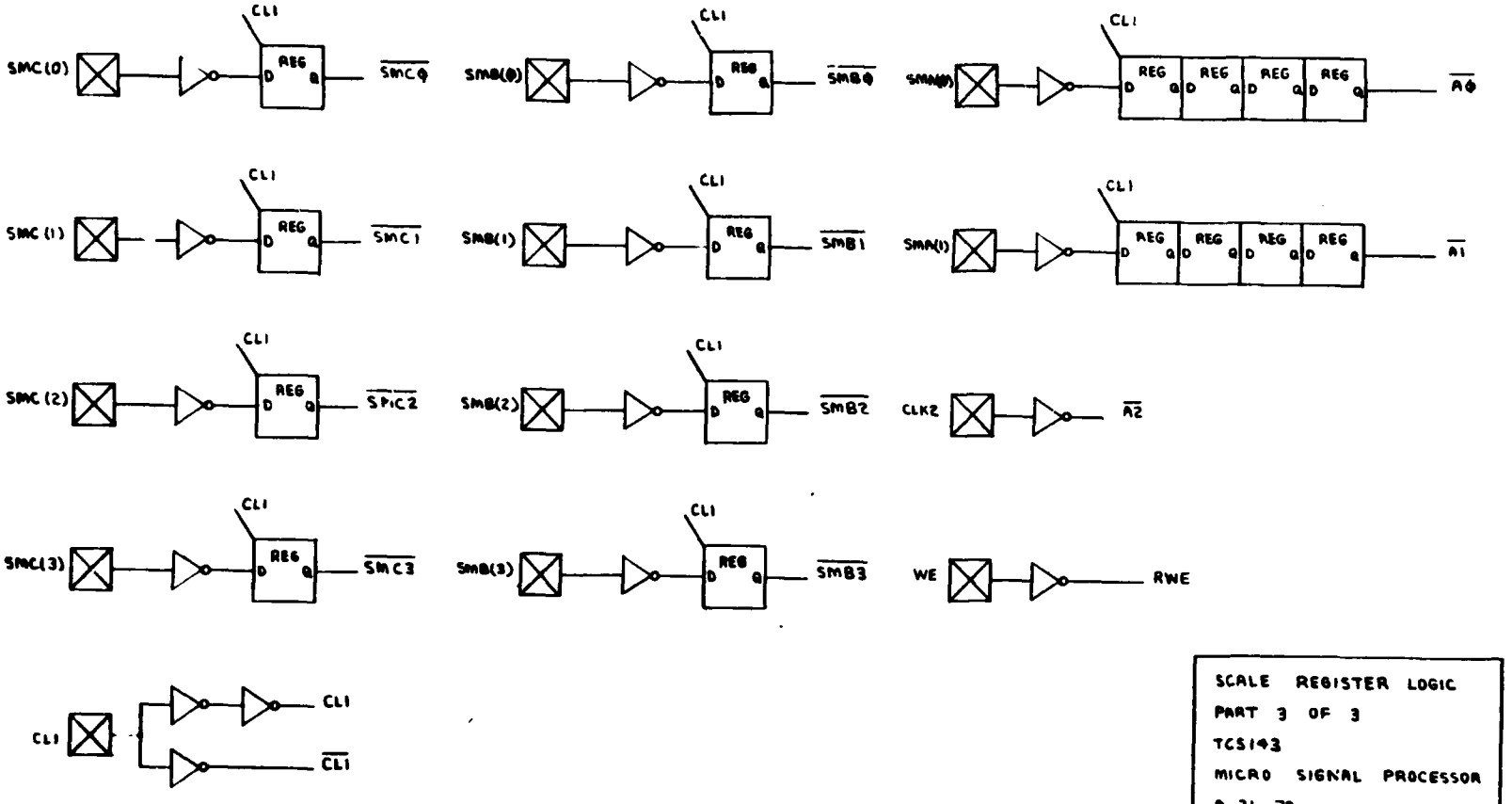


Figure F-4 Scale Register Logic (Part 2)



SCALE REGISTER LOGIC
PART 3 OF 3
TCS143
MICRO SIGNAL PROCESSOR
9-26-78
JIP

Figure F-5 Scale Register Logic (Part 3)

1.4 Shift Count Generator

The shift count generator shown in Fig. F-6 takes the SCO output from the scale register logic and conditionally (dependent on the PM8 input) adds an external five bit shift factor CMSF to this number. When PM8 is low, the output of the adder is CMSF. When PM8 is high, the adder output is CMSF plus SCO. If the output of this adder is positive, it is supplied directly to the shift barrel where it controls the shifting. If the adder output is negative, a factor of 12 is added in making it positive before going to the shift barrel. This guarantees that a positive number requiring only one direction of shifting (left) is always supplied to the shift barrel. To allow compensation whenever the factor of 12 is added in, the sign bit is brought off chip in complemented form as the $\overline{\text{MSA}}$ output.

The CMSF inputs to the array are latched into latches controlled by the clock CB at the chip input. These latches are transparent when CB is low and hold the data when CB is high. A second set of latches, located after the adder, are transparent when CL1 is high and hold data when CL1 is low. Together, these latches function as a retiming register providing CB transitions coincide with CL1 transitions.

1.5 Reorder Delay RAM

The reorder delay RAM shown in Fig. F-7 is a 12 bit by 8 word multiport which is used to store and reorder the input data DATI. The addressing is controlled by the CP input to the chip (Fig. F-8). Data is sequentially written into successive addresses and read out on the two output ports in permuted order as defined in Table F-2. The data is written into the memory whenever the write enable pulse WE2 is low.

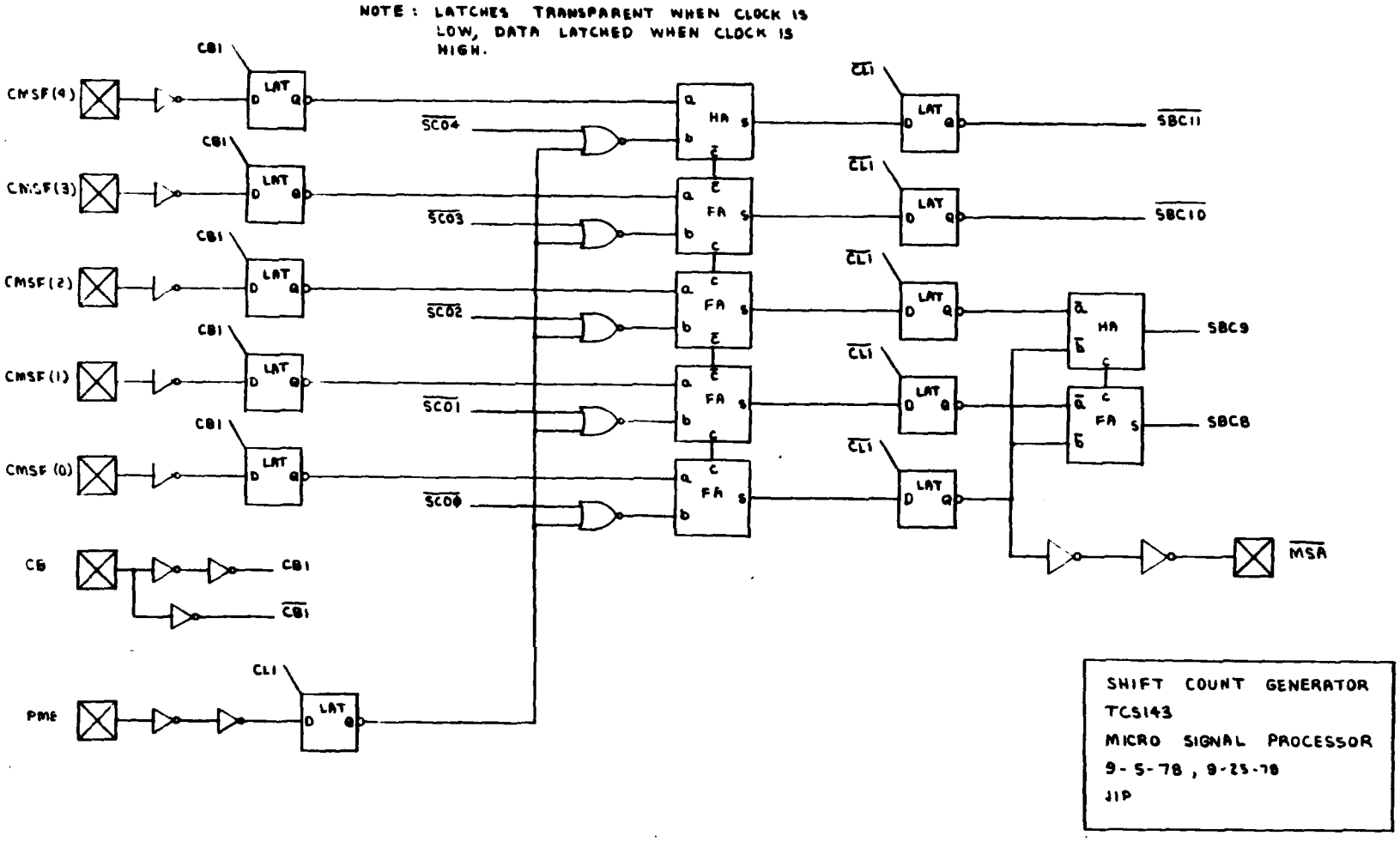


Figure F-6 Shift Count Generator

TABLE F-2

REORDER DELAY RAM ADDRESSING SEQUENCE

Write Address	Read A Address	Read B Address
0	4	6
1	4	6
2	5	7
3	5	7
4	0	2
5	0	2
6	1	3
7	1	3

The two 12 bit outputs are clocked into retiming registers on the positve going edge of the CL1 clock. The output from the A port is labeled L while the output from the B port is labeled M. The L and M together form a 24 bit input to the shift barrel.

Shift Barrel

The logic for the shift barrel is shown in Figs. F-9 through F-13 The inputs to the shift barrel are the four bits from the shift count generator specifying a shift of from 0 to 15 places to the left, and the 24 bits in the L and M outputs from the reorder delay RAM. Prior to reaching the shift barrel proper the L and M data must pass through multiplexers under external control providing prescaling and sign extensions.

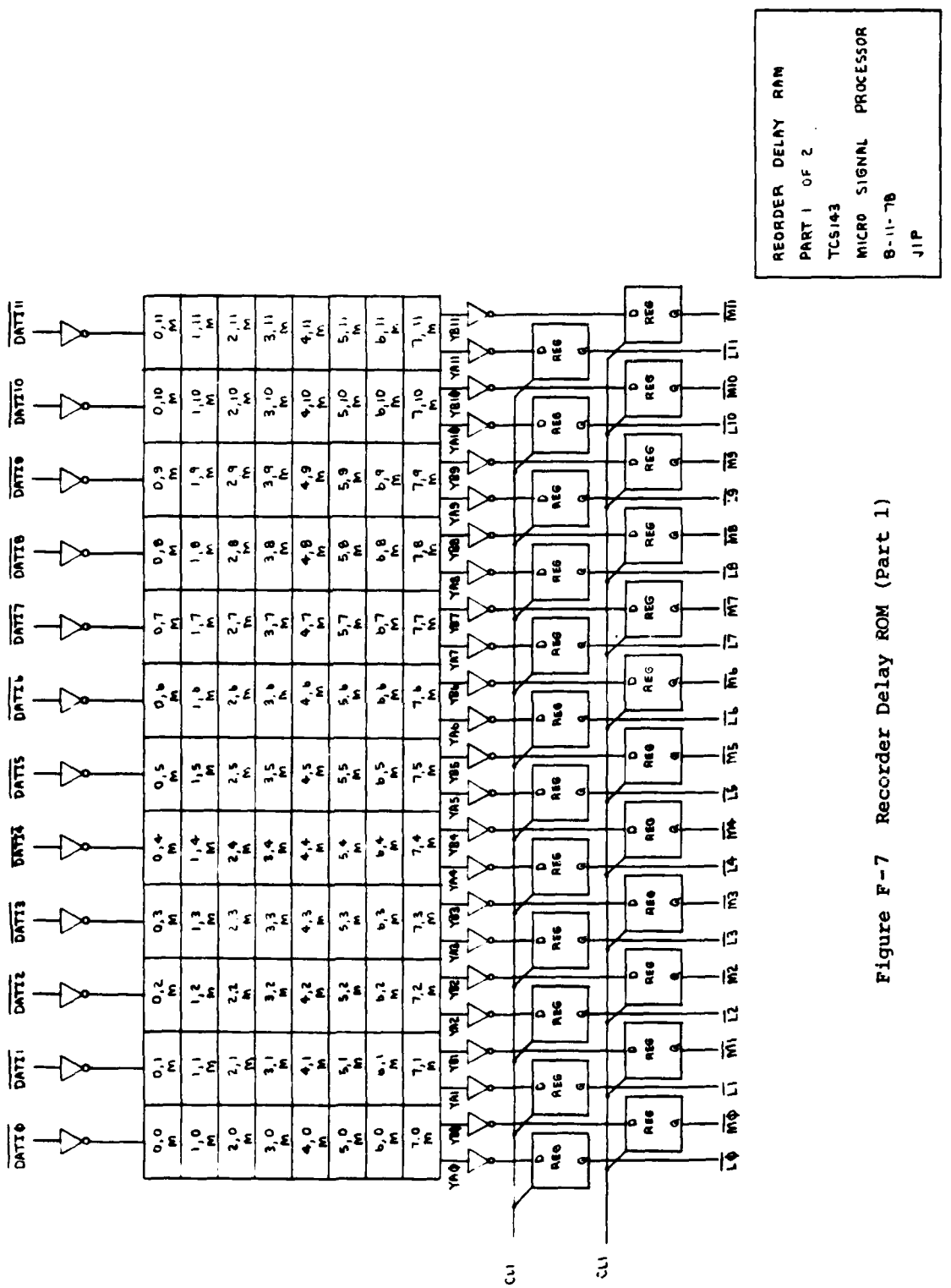


Figure F-7 Recorder Delay ROM (Part 1)

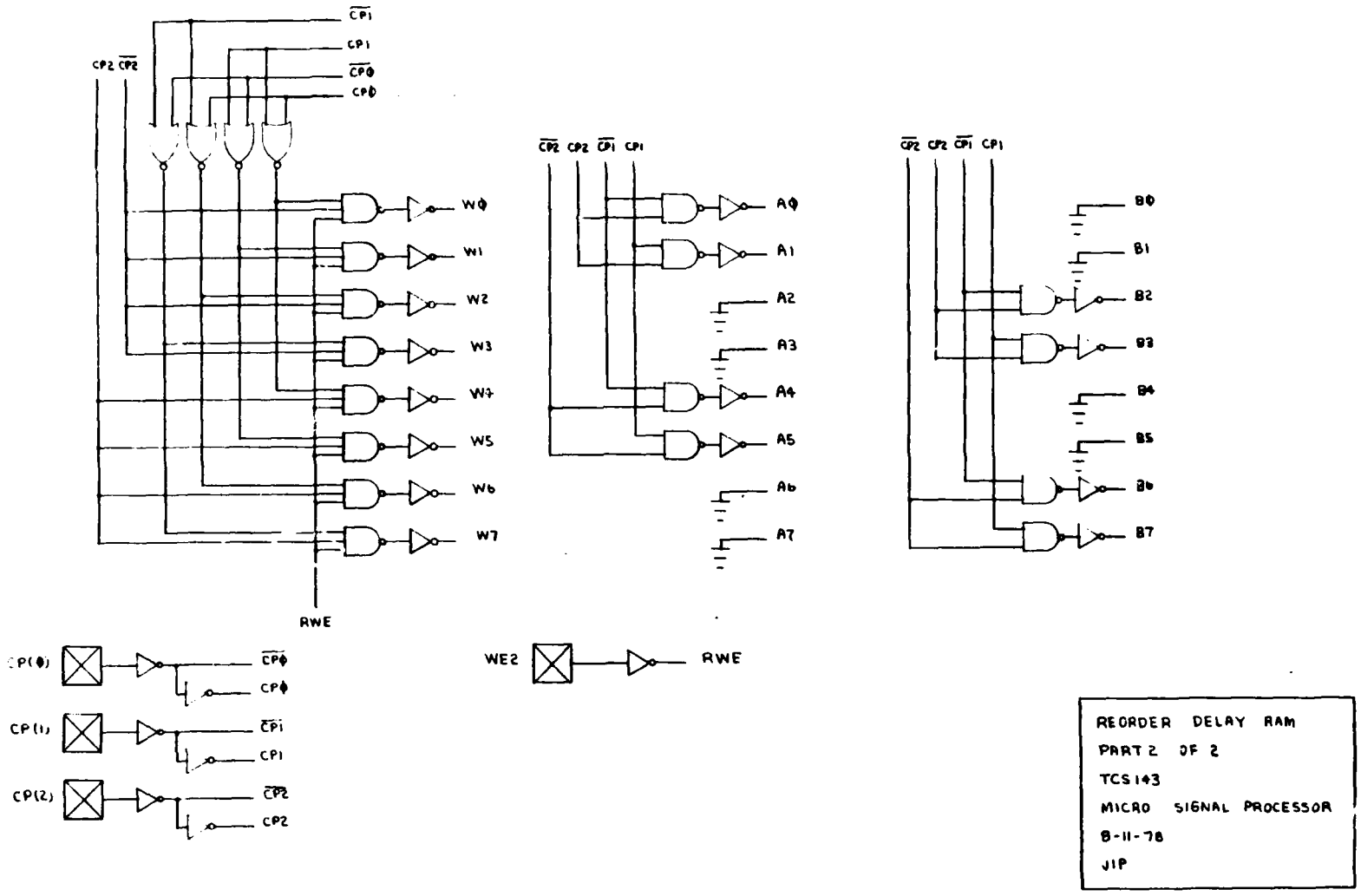


Figure F-8 Recorder Delay RAM (Part 2)

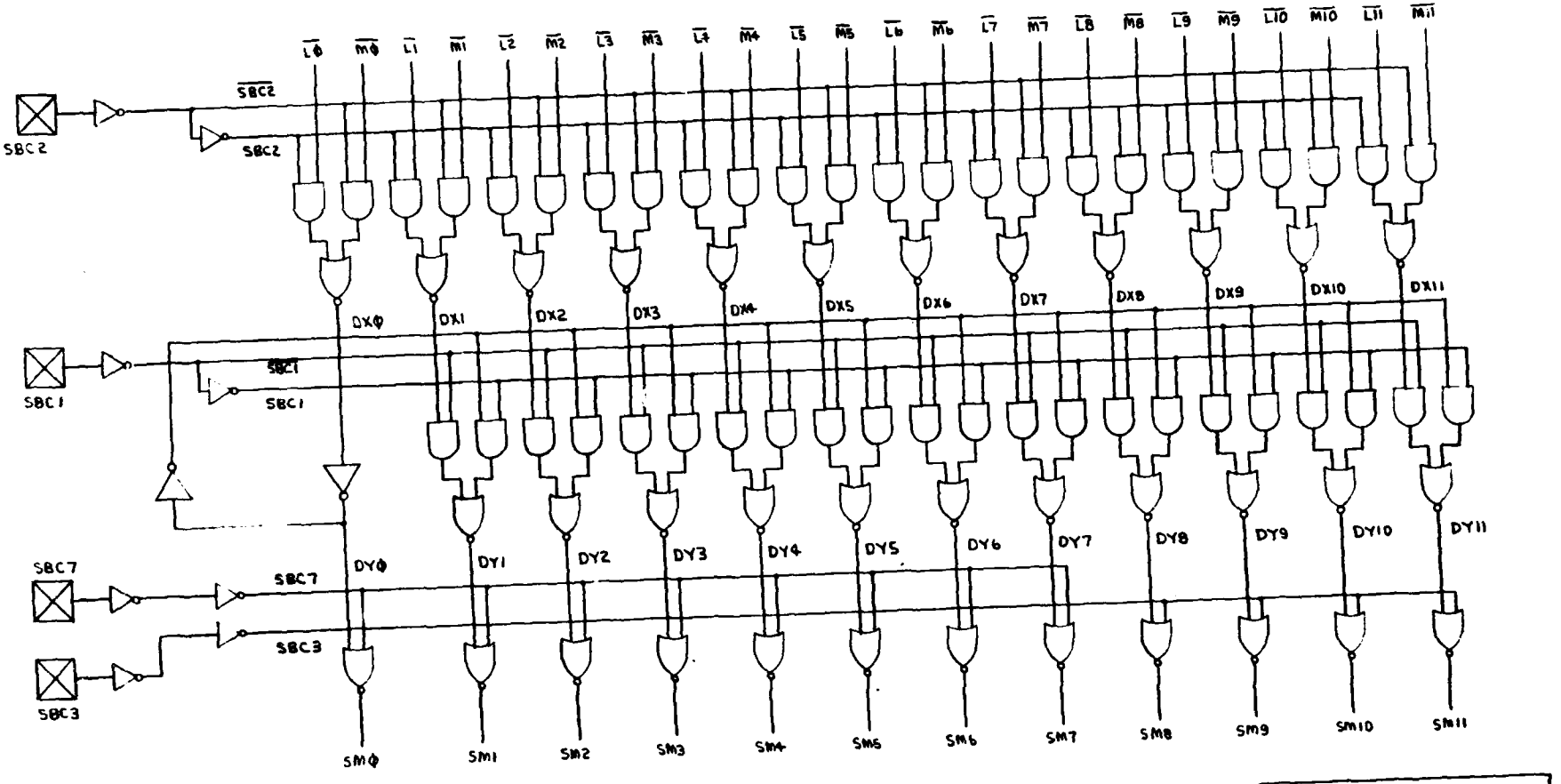
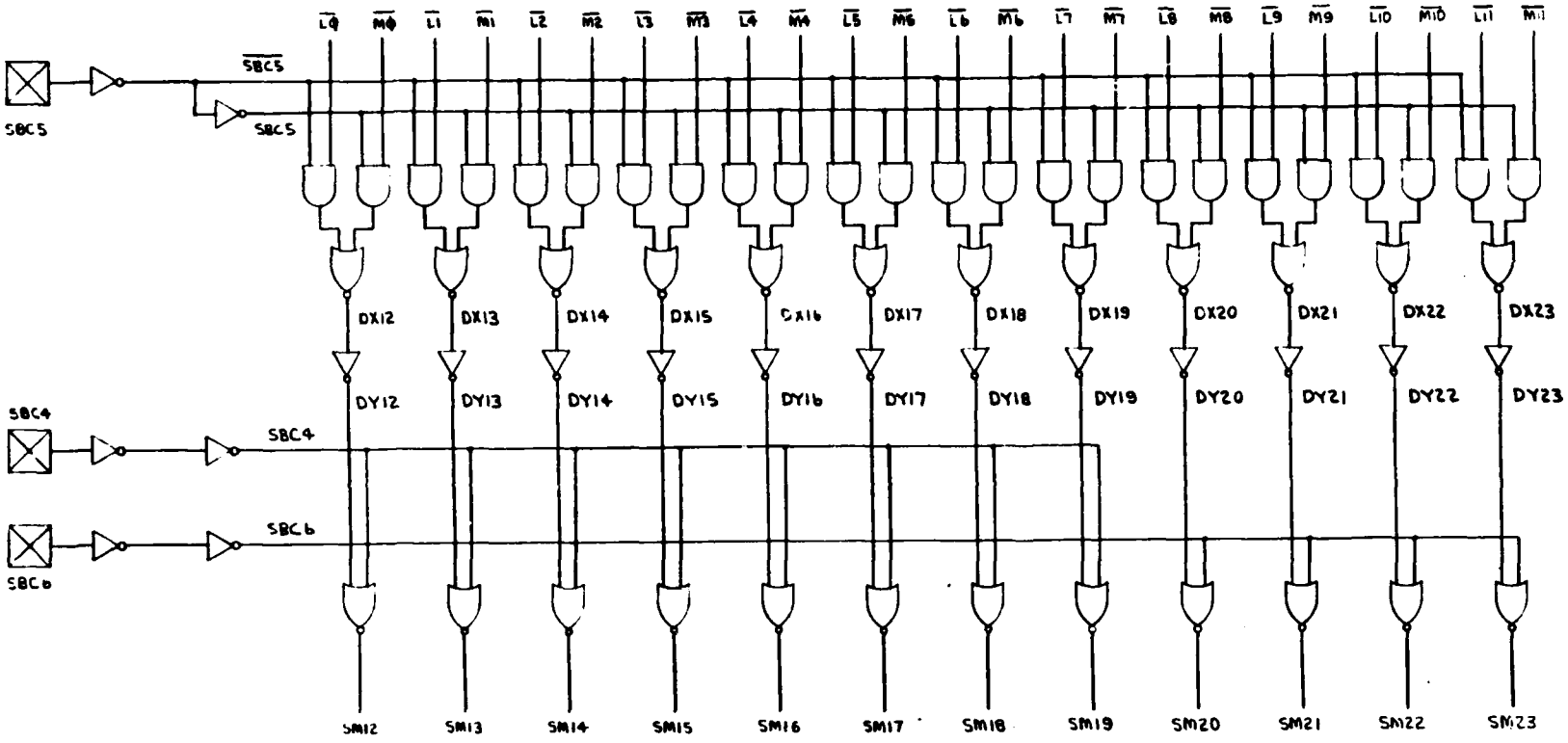


Figure F-9 Shift Barrel (Part 1)



SHIFT BARREL
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TCS143
MICRO SIGNAL PROCESSOR
8-14-78 , 9-22-78
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Figure F-10 Shift Barrel (Part 2)

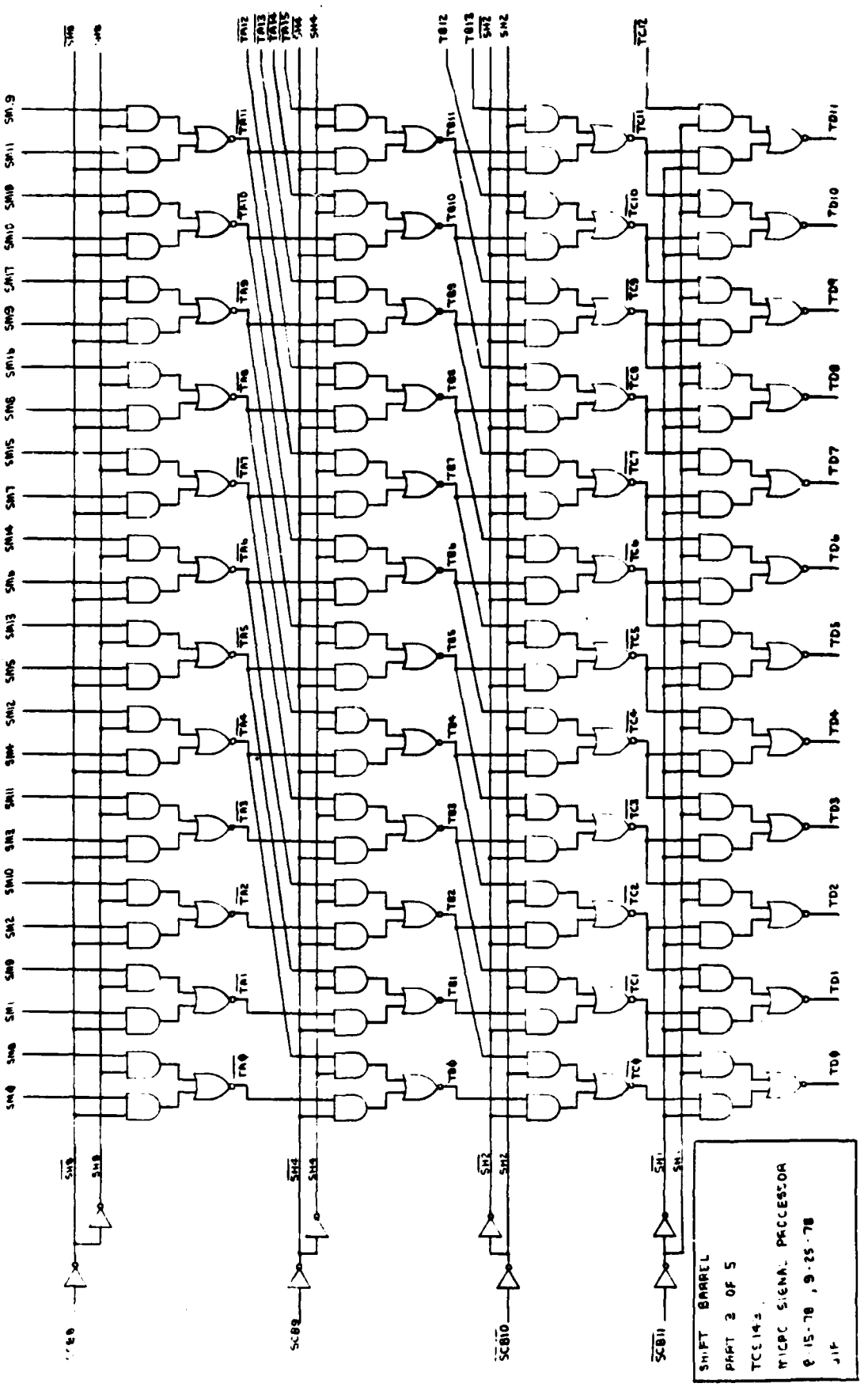
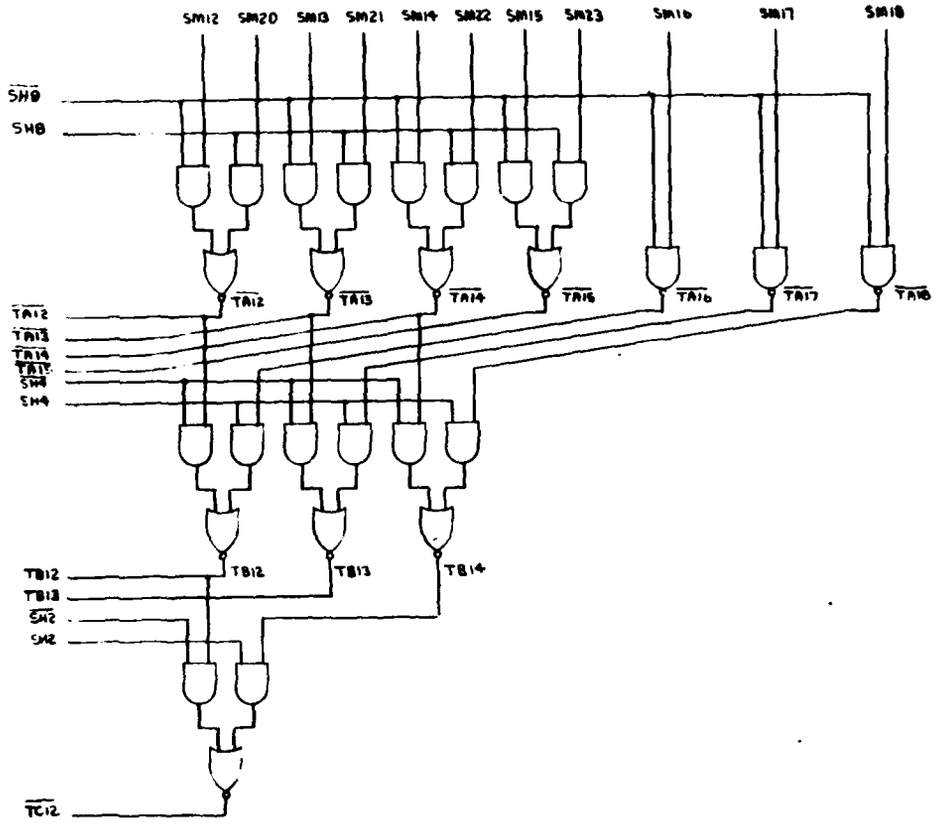


Figure F-11 Shift Barrel (Part 3)



SHIFT BARREL
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TCS143
MICRO SIGNAL PROCESSOR
8-15-78
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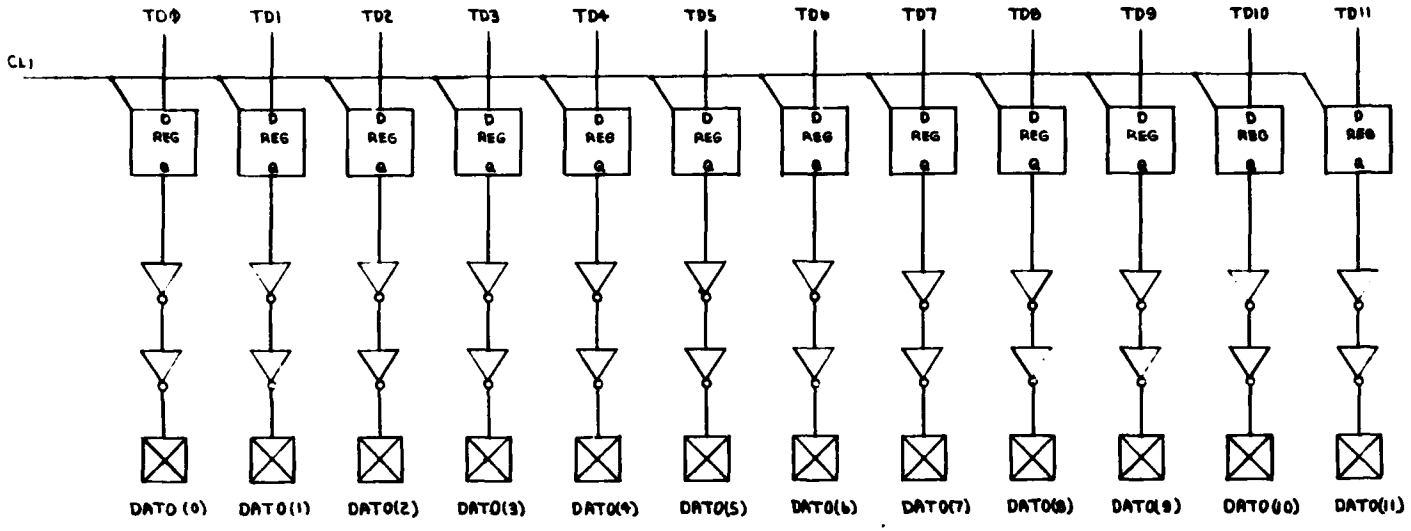
Figure F-12 Shift Barrel (Part 4)



SHIFT BARREL
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TC5143
MICRO SIGNAL PROCESSOR
8-15-78
JIP

Figure F-13 Shift Barrel (Part 5)

The first stage is the definition of the 24 bit input word using the M and L data words and external control signals as defined in Table F-3. In the sign fill the most significant bit of the selected M or L replaces all twelve bits of that word. Using the control inputs the data word can be prescaled in either direction by a factor of 2^{12}.

TABLE F-3

COMPOSITION OF 24 BIT WORD IN THE SHIFT BARREL

Control Inputs			Data Word	
SBC1	SBC2	SBC5	12 MSB	12 LSB
0	0	0	M	L
0	0	1	M	M
0	1	0	L	L
0	1	1	L	M
1	0	0	Sign Fill (M)	L
1	0	1	Sign Fill (M)	M
1	1	0	Sign Fill (L)	L
1	1	1	Sign Fill (L)	M

The next operation allows certain blocks of the data word to be forced to a logic 0 under external control as follows:

SBC6 - 4 least significant bits

SBC4 - next 8 least significant bits

SBC3 - next 4 least significant bits

SBC7 - 8 most significant bits

A high on the control input forces the appropriate block of data bits to 0 while a low allows the data bits to pass unchanged. The output from this operation is the 24 bit word supplied to the shifting network.

The shifting network consists of a bank of multiplexers four deep. In the first level a shift of 8 to the left is made if required, in the second level a shift of 4 to the left is made on the output of the 1st level if required, in the third level a shift of 2 is made if required, and in the final level a shift of 1 place is made if required. The output from the 12 most significant bits is retimed and brought off chip as the DATO output.

1.6 Scaler I/O Signals

Table F-4 is a list of inputs to the scale chip with some descriptive commentary.

TABLE F-4

SCALER I/O SIGNALS

		Number of Signals
1.	V_{DD} - Power Input	1
2.	GND - Power Return	1
3.	CMSF (0-4) - A 5 bit 2's complement number which is optionally added to an internal scale factor in the Shift Count Generator. Bit 0 is the MSB.	5
4.	DATI (0-11) - 12 bit data input. Bit 0 is the MSB. Bits 7-11 are optionally treated as exponents in the Scale Register Logic.	12
5.	WE, WE2 - Write enable signals - Logic 0 = write.	2
6.	CP (0-2) - Address bits for ORDER MEMORY.	3
7.	CL1 - Clock for registers in ORDER MEMORY, Lead Zero Count, Scale Register, and Shift Count Generator.	1
8.	SBC (1-7) - Shift Barrel Controls	7

SBC1	SBC2	Left MUX Out
0	0	M input from ORDER MEMORY
0	1	L input from ORDER MEMORY
1	0	M MSB (extended)
1	1	L MSB (extended)

SBC3 - Logic 1 forces left MUX 4 LSB's to Logic 0; when Logic 0, LSB's are enabled.
SBC4 - Logic 1 forces 8 MSB's of right MUX to 0; when Logic 0, MSB's are enabled.

SBC5	Right MUX Output
0	L input from ORDER MEMORY
1	M input from ORDER MEMORY

SBC6 - Logic 1 forces right MUX 4 LSB's to Logic 0; when Logic 0, LSB's are enabled.
SBC7 - Logic 1 forces left MUX 8 MSB's to Logic 0; when Logic 0, bits are enabled.

9.	CB - Clock for coefficient inputs to Shift Count Generator - Rising Edge Trigger.	1
10.	PMO - Sign bit enable for Lead Zero Count. When Logic 1, sign is enabled; when 0, positive number is assumed.	1
11.	SRC - Select bit for Scale Register Logic. Logic 0 selects Lead Zero Count Input. Logic 1 selects DATI (7-11) exponent input.	1
12.	SRH - Sign bit control for Scale Register Logic input. Logic 1 allows signed input, Logic 0 forces positive number.	1

TABLE F-4

SCALER I/O SIGNALS (CONTINUED)

		Number of Signals
13.	SMA (0-1) - LSB address bits for Scale Register Logic multiport memory read port A.	2
14.	CLK2 - Address bit for Scale Register Memory.	1

A addresses MSB is A3 = Logic 1
to A2 = CLK2
Scale Register A1 = SMA1
Memory
LSB is A0 = SMA0

15.	SMB (0-3) The address for the B read port of the Scale Register multiport memory.	4
16.	SMC (0-3) - The address for the write port of the Scale Register multiprot memory.	4
17. 18. 19.	MXSA MXSB MUX2 Multiplexer control bits for Scale Register Logic. In conjunction with an internal sign bit from a subtract operation these bits control the multiplexer which determines the next multiport input. A truth table is shown below.	3

MUX2	MXSB	MXSA	Internal Sign	MUX Output (Multiport Input)
0	0	X	X	A Input to subtractor (subtractor operation = A - B) is the output from input select MUX.
0	1	0	X	Multiport Feedback (B Outputs)
0	1	1	0	Multiport Feedback (B Output)
0	1	1	1	A See above
1	1	0	X	Subtractor Output
1	1	1	0	Subtractor Output

20.	PM8 - Multiplexer control bit in Shift Count Generator. Logic 0 selects CMSF (0-3) inputs, Logic 1 selects the sum of CMSF (0-3) added to the SCale Register Logic Output.	1
	Total Input Pins	51

Output Definition

Table 5.6.2-2 shows the output signals from the scaler chip.

Table 5.6.2-2. TCS143 Output Signals

		Number of Signals
1.	$\overline{MSA}$ - Sign bit from Shift Count Generator Logic 1 = positive, 0 = negative.	1
2.	DAT0 (0-11) Scaled data outputs to rest of pipeline.	12
	Total Output Pins	13
	Total Pins	64

1.7 Circuit Cell Description

The TCS143 Scaler Array consists of 62 active circuit cells and 32 inactive cells for a total of 95 custom cells. The active cells contain the transistors required to implement the logic while the inactive cells contain array level interconnections and descriptive alphanumerics. Table F-5 lists all the cells along with the individual cell transistors, number of times a particular cell is used, and total array transistors. The TCS143 contains 4810 transistors (devices). Not included in this total count are the transistors associated with two test structures included on the array, namely, a 21 stage ring oscillator and a standard test transistor used to obtain processing information.

Fig. F-14 is a cell map of the TCS143 showing all cell locations. This map may be compared with the composite checkplot shown in Figure F-15.

TABLE F-5

TCS143 CELLS

Cell Number	Name	Number Of Devices	Number of Times Used	Total Devices
D1*	Memory Cell	10	141	1410
D2	Clock Driver	6	1	6
D10	Reorder RAM Address	14	4	56
D11	Reorder RAM Address	14	4	56
D12	Reorder RAM Address	22	1	22
D13	RAM Decode Intcnt.	--	1	--
D14	RAM Decode Intcnt.	--	1	--
D15	5 x 9 W, RA Address	16	9	144
D16	5 x 9 W, RA Intcnt.	--	1	--
D17	5 x 9 RA Drivers	10	1	10
D18	5 x 9 Address Logic	32	1	32
D19	5 x 9 RB Address	8	9	72
D20	Dual Shifter	16	23	368
D21	Single Shifter	8	2	16
D22	Shifter End	--	1	--
D23	Shifter Intcnt.	--	6	--
D24	Shifter Intcnt.	--	6	--
D25	Shifter Intcnt.	--	1	--
D26	Shifter - SH8 - LSB	12	1	12
D27	Shifter Intcnt.	--	6	--
D28	Shifter Intcnt.	--	1	--
D29	Shifter Intcnt.	--	1	--
D30	Full Adder, No $\overline{C_{out}}$	22	1	22
D31	Full Adder, No $\overline{C_{out}}$	22	1	22
D33*	Full Adder, C_{in}, C_{out}	30	3	90
D39	Adders	58	1	58
D43*	Full Adder, $\overline{C_{in}}$, C_{out}	28	4	112
D50	Latch	8	4	32
D51	Latch	8	1	8
D52	PM8 Latch	10	1	10
D53	CMSF Latch	8	5	40
D54	CMSF Latch Clock	6	1	6
D60*	Retimer	16	10	160
D61*	Retimer	16	2	32
D62	SMA Retimer	16	19	304
D63	A0 Retimer	16	1	16
D64	SMA0 Retimer	16	2	32
D70	Output Driver	4	13	52
D81*	Input Circuit	2	26	52
D83*	Input Circuit	2	22	44
D90	Memory Out Buffer	4	12	48
D91	Reorder RAM L Reg.	16	12	192
D92	Reorder RAM M Reg.	16	12	192
D93	Reorder RAM In Buffer	2	12	24
D94	5 x 9 Output Buffer	12	5	60
D95	5 x 9 Output Intcnt.	--	3	--
D96	5 x 9 Output Intcnt.	--	2	--
D97	SC0 Latch/NOR	20	5	100

TABLE F-5

TCS143 CELLS (CONTINUED)

Cell Number	Name	Number Of Devices	Number Of Times Used	Total Devices
D98	MPB Contact	--	1	--
D100	TCS143	--	1	--
D101*	Level Numbers	--	1	--
D103*	PLY	--	1	--
D104*	N+	--	1	--
D105*	CNT	--	1	--
D106*	MET	--	1	--
D107*	PAD	--	1	--
D108*	ILD	--	1	--
D109*	P+	--	1	--
D111*	Alignment, D.F.	--	2	--
D112*	Alignment, L.F.	--	2	--
D113*	Test Transistors	2	1	2
D121	Ring Oscillator, Inv.	2	20	40
D122	Ring Oscillator, Out	6	1	6
D210	MPI Select	14	5	70
D211	Adder Input Logic	8	4	32
D212	SMB Addr. Logic	14	1	14
D213	SMB Addr. Logic	8	1	8
D214	Adder Input Logic	6	1	6
D215	SRC1 Buffers	4	1	4
D216	Select Control 1	6	1	6
D217	Select Control 2	10	1	10
D218	Select Control 3	10	1	10
D220	Dual NOR	8	12	96
D221	Dual NOR Input	--	4	--
D222	Dual NOR Input	--	8	--
D223	Shifter Intcnt.	--	1	--
D224	Shifter Intcnt.	--	1	--
D225	Shifter Intcnt.	--	1	--
D226	Select/Inverter	10	11	110
D227	Dual Select	16	12	192
D228	Shifter Intcnt.	--	1	--
D229	Shifter Intcnt.	--	1	--
D230	Shifter Intcnt.	--	1	--
D231	Shift Drivers	14	1	14
D232	Dual Select Inverter	2	1	2
D233	DX0 Inverter	4	1	4
D234	SH1, SH2 Driver	4	2	8
D235	Dual Shifter	16	4	64
D240	Priority Encoder	30	3	90
D241	Lead Zero Input Sel.	8	11	88
D242	Lead Zero Input Sel.	8	1	8
D243	Lead Zero Output	54	1	54
D244	Lead Zero Input Control	2	1	2
D245	Lead Zero Input Control	6	1	6

TABLE F-5

TCS143 CELLS (CONTINUED)

Cell Number	Name	Number Of Devices	Number Of Times Used	Total Devices
D191	Array Intcnt.	--	1	--
D192	Array Intcnt.	--	1	--
D193	Array Intcnt.	--	1	--
D194	Array Intcnt.	--	1	--
D195	Array Intcnt.	--	1	--
D196	Array Intcnt.	--	1	--
			Total Devices**	4810

*Common cells to TCS140 & TCS142.

**Total devices for array does not include test transistors or ring oscillator.

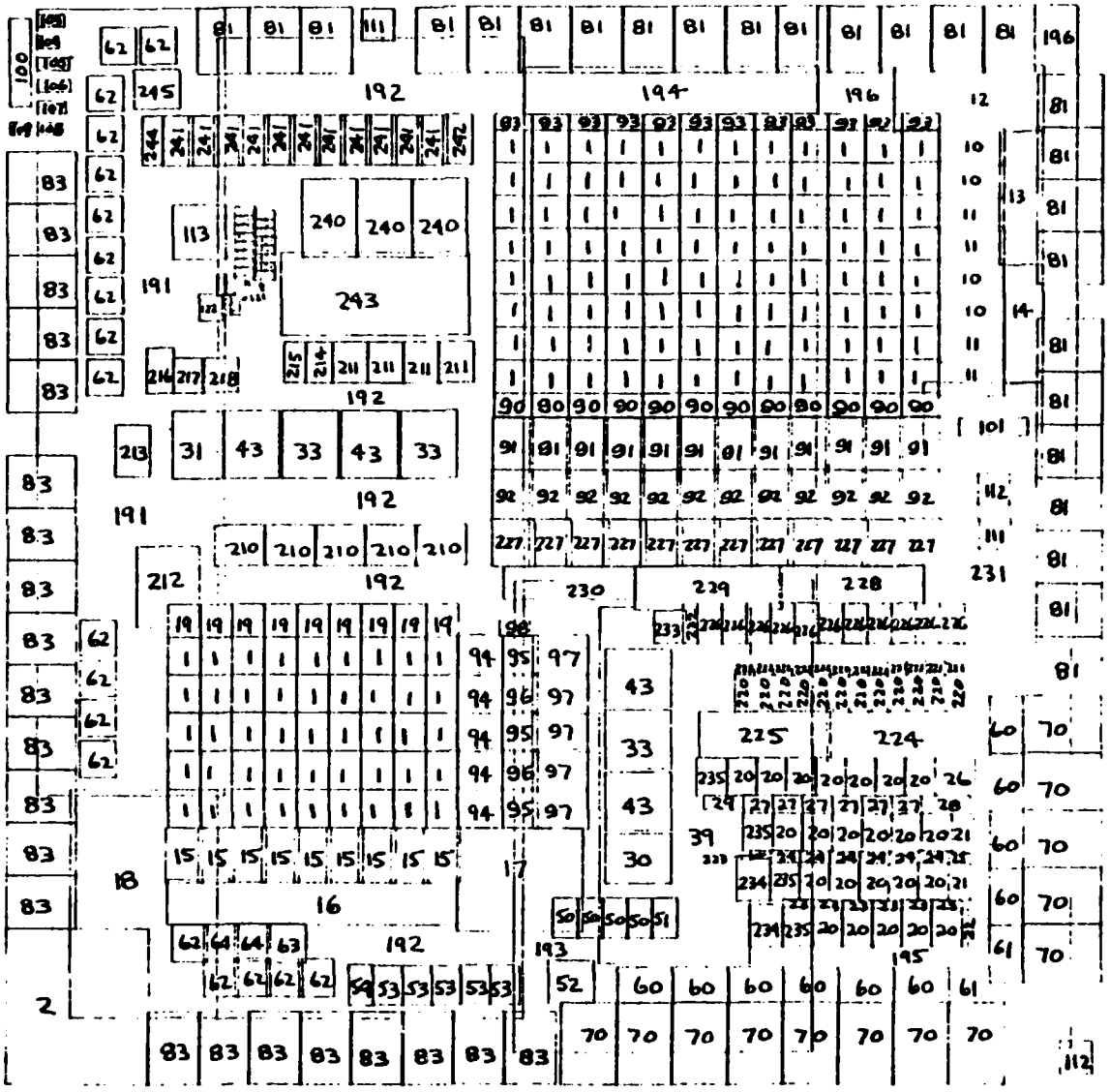


Figure F-14 Cell Drop for TCS143

1.8 Design Specification

The design specifications for the TCS143 are shown in Tables F-6 and F-7.

The static characteristics shown in Table F-6 are shown for both 5V and 10V operation. The array has been designed to operate over the temperature range of -55°C to +125°C. The prime operation of this array will be in a 10V system.

Table F-7 shows the switching characteristics for the array. Table F-8 lists the required propagation delays for the various circuit functions.

TABLE F-6

STATIC SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range Operating	$-55^{\circ}C$ to $+125^{\circ}C$
Non-operating	$-65^{\circ}C$ to $+150^{\circ}C$
Supply Voltage	+15V non-operating
Input Voltage	-.5V to Vcc +.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	Vcc	LIMITS MIN	TYP	MAX	UNITS
Icc Quiescent Current	10V	-	-	~~250~~ 250	µamp
VOL Output Low	any	-	.05	.1	Volt
VOH Output High	any	Vcc-.1	Vcc-.05	-	Volt
VIL Input Low	5 10	-	-	1.5 3.0	Volts
VIH Input High	5 10	3.5 7.0	-	-	Volts
IO Outputs Sink and Source	5 10	-	1.5 within .5V of Supply or GND 1.5 within .5V of Supply or GND		ma
Iin Input Current	$0 \leq E_{IN} \leq V_{cc}$	-	.3	.1	µamp
Cin data/clock	any	-	2	3/5	pf
Vcc	-	4.5	10	12	Volts

TABLE F-7

SWITCHING CHARACTERISTICS

CHARACTERISTICS	Vcc	MIN	TYP	MAX	UNITS
OUTPUT RISE AND FALL TIME (15pf load)	5 10	-	30 15	40 18	nsec nsec
DATA SETUP TIME	10	-	5	7	nsec
DATA HOLD TIME	10	-	8	10	nsec
CLOCK WIDTH	any	50	75	-	nsec
CLOCK RATE	5 10	 6.66	3.0 6.66	-	MHZ MHZ
CLOCK TO OUTPUT(REGISTER)	10	-	15	20	nsec
PD @6.6 MHZ	10	-	-	300	mW

TABLE F-8

TIMING CHARACTERISTICS

	MIN	TYP (nsec)	MAX (nsec)
I. - Reorder Memory			
1. Write Pulse Width	-	50	50 nsec
2. Access Time (from Write Pulse Leading Edge enable into register includes setup).	-	40	50 nsec
II. - Scale Register Logic			
1. Data In through Lead Zero Count to Multiport Write	-	120	150 nsec
2. Multiport Read to Write Write via subtract and MUX (Feedback Path) -	-	70	80 nsec
3. Multiport Access Time	-	40	50 nsec
III. - Shift Count Gen			
Data In to Data Out (Worst Case) path	-	25	50 nsec
IV. - Shift Barrel			
Control to correct output	-	50	70 nsec
Data In to Data Out	-	50	70 nsec

1.9 Test Word Generation

The final design of the TCS143 possesses three characteristics that made creating a test sequence for the array an extremely involved and time consuming task. First, the large size of the array (almost 5000 devices) necessitated a long test word to ensure that most of the devices would be exercised. Second, the timing relationships of the inputs to the array required a multistep clocking process in the test word so that the test data would satisfy expected system timing. Finally, the large ratio of array inputs (49) to outputs (13) resulted in some of the logic being inaccessible to direct testing and several steps were required to route test signals through these areas of the array.

The magnitude of the problems mentioned above was reduced by using the TESTGEN program to simulate the operation of the TCS143 and evaluate the effectiveness of the selected test patterns. The array model for TESTGEN purposes was derived by partitioning the TCS143 logic into six subsections called "macros" and modeling each macro separately. TESTGEN simulations of each macro were used to verify the accuracy of the logic before interconnecting the macros to form the TESTGEN model for the complete array.

The macro concept was also utilized to simplify generating the test patterns that are contained in the TCS143 test word. Input patterns to the array were arranged so that at any point in the test sequence, only one of the six logic sections would be permitted to affect the thirteen outputs of the TCS143. This procedure confined the problem of choosing effective test patterns to a small and functionally homogenous area of the chip rather than testing several regions and operations simultaneously.

The test word that resulted from this effort contains 774 steps or patterns in the form of 258, three step clock cycles. The 774 steps do not include the "walking 1's" or "walking 0's" tests because adding them would require at least an additional 500 steps. Instead, the RAM portions of the array are exercised by writing and reading all 1's, all 0's, and alternating 1's and 0's.

1.10 Physical Characteristics

Figure F-15 is a composite checkplot of the final layout configuration of the TCS143. Comparison with the cell map of Section 1.7 will indicate the main register stack areas. All seven layers required by the process are included in this plot.

The array size is 214 mils x 206 mils and contains 4810 transistors. The array sizing factor is 9.2 sq. mils per device. This factor indicates that the TCS143 is slightly more dense than the TCS142. There are more transistors sharing the overhead area on the TCS 143 and, in addition, the output drivers are fewer and smaller on the TCS143.

The 51 active leads require use of a 64 lead package. Again, this array will use the 64 lead DIC or the 64 pin LHP as discussed previously for the TCS140. A bonding diagram is shown in Figure F-16 and Table F-9 shows the package pins for each signal.

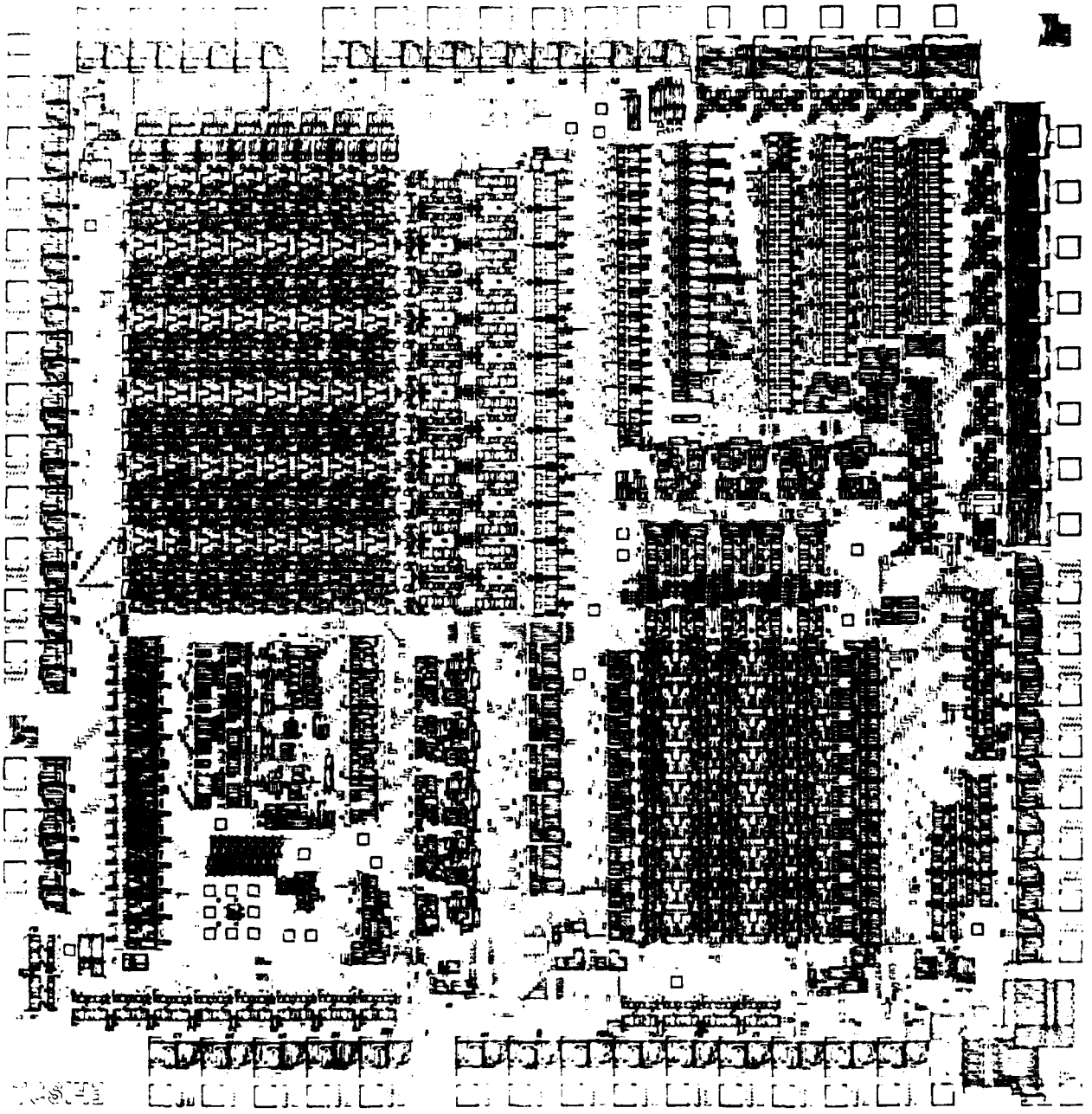


Figure F-15 Composite Checkplot Diagram

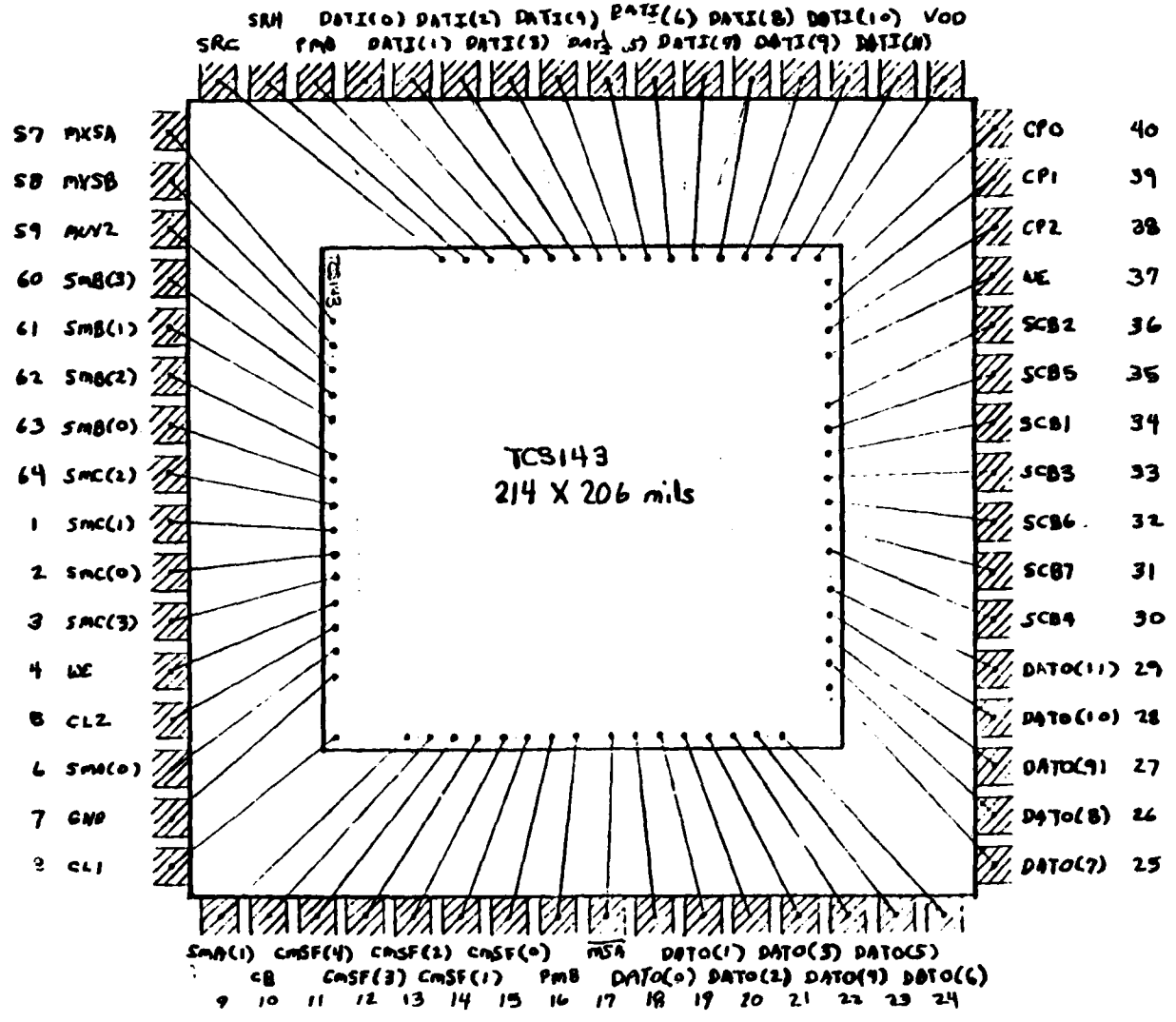
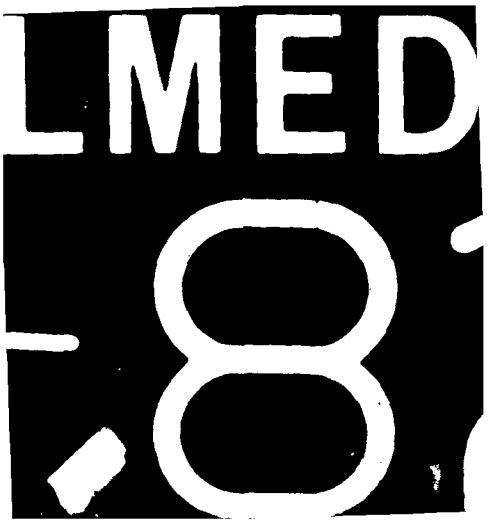


Figure F-16 CS43 Bonding Diagram

TABLE F-9

TCS143 PINOUTS

Pin #	Signal Name	Pin #	Signal Name
1	SMC(1)	33	SCB3
2	SMC(0)	34	SCB1
3	SMC(3)	35	SCB5
4	WE	36	SCB2
5	CL2	37	WE2
6	SMA(0)	38	CP2
7	GND	39	CP1
8	CL1	40	CP0
9	SMA(1)	41	VDO
10	CB	42	DATI(11)
11	CMSF(4)	43	DATI(10)
12	CMSF(3)	44	DATI(9)
13	CMSF(2)	45	DATI(8)
14	CMFS(1)	46	DATI(7)
15	CMSF(0)	47	DATI(6)
16	PM8	48	DATI(5)
17	MSA	49	DATI(4)
18	DATO(0)	50	DATI(3)
19	DATO(1)	51	DATI(2)
20	DATO(2)	52	DATI(1)
21	DATO(3)	53	DATI(0)
22	DATO(4)	54	PM0
23	DATO(5)	55	SRH
24	DATO(6)	56	SRC
25	DATO(7)	57	MXSA
26	DATO(8)	58	MXSB
27	DATO(9)	59	MUX2
28	DATO(10)	60	SMB(3)
29	DATO(11)	61	SMB(1)
30	SCB4	62	SMB(2)
31	SCB7	63	SM3(0)
32	SCB6	64	SMC(2)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